Our Docket No.: 0325.00503

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Applicant	James H. Lie.		
Application No.:	09/940,749	Examiner:	Thompson, A.
Filed:	August 28, 2001	Art Group:	2825

For: METHOD AND/OR ARCHITECTURE FOR GENERATING SUPERSET PINOUT FOR DEVICES WITH COMBINED PROGRAMMABLE LOGIC AND HIGH-SPEED SERIAL CHANNELS

I hereby certify that this letter, the response or amendment attached hereto are being deposited with the United States Postal Service as first class mail in an envelope addressed to Mail Stop Appeal Brief Patent, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on September 1, 2004.

By: Jan M. Dunbar
Jan M. Dunbar

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. §1.192 for consideration by the Board of Patent Appeals and Interferences. Appellants also submit herewith a PTO-2038 Form in the amount of $440.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §1.17(c) and a one-month extension. Please charge any additional fees or credit any overpayment to our Deposit Account Number 50-0541.

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Claim Summary

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I. REAL PARTY IN INTEREST

The real party in interest is the Assignee, Cypress Semiconductor Corporation.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Appellant, Appellant's legal representative, or Assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-4, 6-11 and 13-20 are pending and remain rejected. Claims 1-3, 9-11, 18-20 were amended subsequent to the final rejection. The Appellant hereby appeal the rejection of claims 1-4, 6-11 and 13-20. A claim summary, which reflects the claims as amended, is attached in the Appendix.

IV. STATUS OF AMENDMENTS

Appellant is appealing a final Office Action issued by the Examiner on December 30, 2003.[1] On March 22, 2004, Appellant filed an Amendment After Final that amended claims 1-3, 9-11 and 18-20. In an Advisory Action dated May 12, 2004, the Examiner entered the Amendment After Final, but maintained the rejections of claims 1-20.[2] On May 27, 2004, Appellants filed a second Amendment After Final along with a Notice of Appeal. The Notice of Appeal was received

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[1] Paper no. 5.

[2] See item 3 on page 2 of paper no. 050604.

in the U.S. Patent and Trademark Office on June 1, 2004. In an Advisory Action dated July 12, 2004, the Examiner stated that the second Amendment After Final would not be entered. In an Advisory Action dated August 11, 2004, the Examiner again stated that the second Amendment After Final would not be entered.

V. SUMMARY OF INVENTION

In a first embodiment, the present invention provides a method for generating a superset pinout for a family of devices (FIGS. 1a and 1b and page 6, lines 10-16 and page 10, lines 7-8 of the specification), comprising the steps of: (A) defining a pinlist for each device within the family of devices (Element 52 in FIGS. 1a and 1b and page 6, lines 1-9 and 17-18), (B) generating a superset listing of pins from the pinlist (Elements 54 and 54' in FIGS. 1a and 1b and page 7, lines 6-11), (C) creating the superset pinout for the family of devices from the superset listing of pins to eliminate potential footprint variations within the family of devices (Element 56 in FIGS. 1a and 1b and page 7, line 12 through page 8, line 16) and (D) marking each pin of the superset pinout associated with each member of the family of devices (FIGS. 1a, 1b, 2 and 3 and page 8, lines 3-16).

In a second embodiment, the present invention provides an apparatus for generating a superset pinout for a family of devices comprising: (i) means for defining a pinlist for each device within the family of devices (Element 52 in FIGS. 1a and 1b, page 6, lines 10-16 and page 12, line 5 through page 13, line 6 of the specification), (ii) means for generating a superset listing of pins from the pinlist (Elements 54 and 54' in FIGS. 1a and 1b, page 7, lines 6-11 and page 12, line 5 through page 13, line 6 of the specification), (iii) means for creating the superset pinout for the family of devices from the superset listing of pins, where the superset pinout eliminates layout

variations within the family of devices (Element 56 in FIGS. 1a and 1b, page 7, line 12 through page 8, line 16 and page 12, line 5 through page 13, line 6 of the specification) and (iv) means for marking each pin of the superset pinout associated with each member of the family of devices (FIGS. 1a, 1b, 2 and 3, page 8, lines 3-16 and page 12, line 5 through page 13, line 6 of the specification).

In a third embodiment, the present invention provides an apparatus comprising: (i) a device configured to generate a superset pinout for a family of devices (page 12, line 5 through page 13, line 6 of the specification), where (A) the device is further configured to (i) define a pinlist for each device within the family of devices (Element 52 in FIGS. 1a and 1b, page 6, lines 10-16 and page 12, line 5 through page 13, line 6 of the specification), (ii) generate a superset listing of pins from the pinlist (Elements 54 and 54' in FIGS. 1a and 1b, page 7, lines 6-11 and page 12, line 5 through page 13, line 6 of the specification), (iii) create the superset pinout for the family of devices from the superset listing of pins (Element 56 in FIGS. 1a and 1b, page 7, line 12 through page 8, line 16 and page 12, line 5 through page 13, line 6 of the specification), and (iv) mark each pin of the superset pinout associated with each member of the family of devices (FIGS. 1a, 1b, 2 and 3, page 8, lines 3-16 and page 12, line 5 through page 13, line 6 of the specification), and (B) the superset pinout is configured to reduce layout and footprint changes on a board configured to connect to each member of the family of devices (page 10, line 14 through page 11, line 15).

VI. ISSUES

The issue is whether claims 1-4, 6-11 and 13-20 are patentable under 35 U.S.C. §112, second paragraph.

VII. GROUPING OF CLAIMS

Appellant contends that the claims 1-4, 6-11 and 13-20 of the present invention, which are subject to a common rejection, do not stand or fall together. In particular, the following groups of claims are separately patentable:

Group 1: Claims 1-4, 6-9, 11 and 13-18 stand together.

Group 2 Claim 10 stands alone.

Group 3: Claim 19 stands alone.

Group 4: Claim 20 stands alone.

The claim(s) in each group is(are) separately patentable from the claim(s) in any other groups. Arguments in support of each group being separately patentable and the reasons why the Examiner's rejection should be reversed are presented below in the Arguments (See MPEP §1206).

VIII. ARGUMENTS

A. Selected groupings of claims 1-4, 6-9, 11 and 13-20 are each patentable under 35 U.S.C. §112, second paragraph, as (i) setting forth the subject matter that Appellants regard as their invention and (ii) particularly pointing out and distinctly defining the metes and bounds of the subject matter that will be protected by the patent grant.

35 U.S.C. §112, Second Paragraph

As set forth on page 2 of the final Office Action,[3] claims 1-20 are rejected under 35 U.S.C. §112, second paragraph.[4]

The second paragraph of 35 U.S.C.112 is directed to requirements for the claims:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

There are two separate requirements set forth in this paragraph: (A) the claims must set forth the subject matter that applicants regard as their invention and (B) the claims must particularly point out and distinctly define the metes and bounds of the subject matter that will be protected by the patent grant.[5] The first requirement is a subjective one because it is dependent on what the Applicants for a patent regard as their invention. The second requirement is an objective one because it is not dependent on the views of an Applicant or any particular individual, but is evaluated in the context

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[3] Dated December 30, 2003.

[4] See paragraph nos. 5 and 6 on pages 2-3 of the final Office Action dated December 30, 2003.

[5] Manual of Patent Examining Procedure (MPEP), 8th Edition, Rev. 2, May 2004, §2171.

of whether the claim is definite (i.e., whether the scope of the claim is clear to a hypothetical person possessing the ordinary level of skill in the pertinent art).[6]

In a rejection based on 35 U.S.C.§112, second paragraph, the Examiner should further explain whether the rejection is based on indefiniteness or on the failure to claim what Applicants regard as their invention.[7] The content of Applicant's specification is not used as evidence that the scope of the claims is inconsistent with the subject matter which Applicants regard as their invention. As noted in *In re Ehrreich*,[8] agreement, or lack thereof, between the claims and the specification is properly considered only with respect to 35 U.S.C.112, first paragraph; it is irrelevant to compliance with the second paragraph of that section.

1. Group 1 (claims 1-4, and 6-11 and 13-18) is fully patentable under 35 U.S.C. § 112, second paragraph.

The presently pending claim 1 provides a method for generating a superset pinout for a family of devices, comprising the steps of: (A) defining a pinlist for each device within the family of devices, (B) generating a superset listing of pins from the pinlist, (C) creating the superset pinout for the family of devices from the superset listing of pins to eliminate potential footprint variations within the family of devices and (D) marking each pin of the superset pinout associated with each member of the family of devices. Claims 2-4, 6-9, 11 and 13-18 depend, either directly or indirectly, from claim 1.

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[6] *Id.*

[7] MPEP §2171, citing *Ex parte Ionescu*, 222 USPQ 537, 539 (Bd. App. 1984).

[8] 590 F.2d 902, 200 USPQ 504 (C.C.P.A. 1979).

The Examiner failed to explicitly state whether the rejection of claims 1, 2, 4, 6-9, 11 and 13-18 under 35 U.S.C. §112, second paragraph, is based on the failure to claim what the Appellants regard as their invention or on indefiniteness.[9] Therefore, both prongs are addressed for completeness. With regard to claim 3, the Examiner stated that "Applicant fails to set forth the subject matter that Applicant claims as his invention."[10] Whether the claims set forth the subject matter regarded by the Appellants as their invention is a subjective test that is satisfied as evidenced by the submission of claims 1-4, 6-11 and 13-18 for examination. The Examiner failed to present any evidence or convincing line of reasoning to support her position that the invention set forth in the claims is not what the Appellants regard as their invention.[11] The invention set forth in the claims **must be presumed, in the absence of evidence to the contrary, to be that which Appellants regard as their invention.**[12] Since the Examiner presented no evidence or convincing line of reasoning to doubt the invention set forth in the claims is what the Appellants regard as their invention, the presumption that the claims are directed to that which the Applicants regard as their invention is intact. As such, the claims of group 1 are patentable under the first prong of 35 U.S.C. §112, second paragraph, and the rejection should be reversed.

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[9] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604).

[10] See last two lines of paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604).

[11] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604).

[12] MPEP §2172(I), citing *In re Moore*, 439 F.2d 1232, 169 USPQ 236 (C.C.P.A. 1971).

With regard to the second requirement above, the claim 1 step (C) of "creating said superset pinout for said family of devices from said superset listing of pins to eliminate potential variations within said family of devices" meets the objective test of defining the metes and bounds of the subject matter by reciting that a superset pinout is created along with an explanation of what the superset pinout does. The Examiner's conclusory statement that claim 1 is "incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections" where the "omitted structural cooperative relationship" is "the relation between *eliminating footprint variations* and the remainder of the claim 1,"[13] does not provide any analysis of why the scope of the claims of group 1 would not be clear to **a person possessing the ordinary level of skill in the pertinent art when read in light of the specification**.[14] In rejecting a claim under the second paragraph of 35 U.S.C. §112, it is incumbent on the Examiner to establish that one of ordinary skill in the pertinent art, when reading the claims in light of the supporting specification, would not have been able to ascertain with a reasonable degree of precision and particularity the particular area set out and circumscribed by the claims.[15]

The statement by the Examiner that the claims are "incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the

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[13] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604).

[14] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604). See also MPEP § 2173.02.

[15] *Ex parte Wu*, 10 USPQ2d 2031, 2033 (B.P.A.I. 1989) (citing *In re Moore*, 439 F.2d 1232, 169 USPQ 236 (C.C.P.A. 1971); *In re Hammack*, 427 F.2d 1378, 166 USPQ 204 (C.C.P.A. 1970)).

necessary structural connections"[16] clearly does not adequately address, *inter alia*, (i) what is considered to be the pertinent art, (ii) what the level of skill is in the pertinent art and (iii) why **one of ordinary skill in the pertinent art, when reading the claims in light of the specification, would not have been able to reasonably ascertain the specific area set out and circumscribed by the claims**. It is not essential to a patentable combination that there be interdependency between the elements of the claimed device or that all the elements operate concurrently toward the desired result.[17] Furthermore, a claim does not necessarily fail to comply with 35 U.S.C. §112, second paragraph where the various elements do not function simultaneously, are not directly functionally related, do not directly intercooperate, and/or serve independent purposes.[18] Therefore, the Examiner failed to meet the Office's burden of factually supporting a *prima facie* conclusion that the present claims are not definite. As such, the presently pending claims of group 1 are fully patentable under the second prong of 35 U.S.C. §112, second paragraph, and the rejection should be reversed.

Furthermore, one of ordinary skill in the art when reading the claims in light of the specification would clearly understand the relationship between the steps of claim 1. Specifically, the meaning of the terms used in the claims is clearly apparent from the prior art or from the specification and drawings as originally filed. In particular, variations would be understood to refer

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[16] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003.

[17] MPEP § 2171.01, citing *Ex parte Nolden*, 149 USPQ 378, 380 (Bd. Pat. App.1965).

[18] MPEP § 2171.01, citing *Ex parte Huber,* 148 USPQ 447, 448-49 (Bd. Pat. App. 1965).

to changes, differences, dissimilarities, etc.[19] With respect to the terms "pinout" and "pinlist," the specification states:

> **Pinout** may refer to a layout of the signals for a device (e.g., a list of physical pins of a device package and functions assigned to those pins). For example, a pinout may be a list of pins and pin functions for quad flat pack (QFP) (e.g., pin1 = ground, pin2 = signal A, etc.) and for a ball grid array (BGA) (e.g., A1=Ground, A2 = signal A, etc.) **Pinlist** may refer to a list of signals for a device to be assigned to physical pins to become the functions of the pins (e.g., the ground, signal A, etc.). For simplicity a BGA ball may also be referred to as a pin (page 6, lines 1-9 of the specification, emphasis added).

With respect to the term "footprint," one of ordinary skill in the art would recognize the term "footprint", with respect to a device, to refer to the physical pinout or pattern of pins (or balls) of the device.[20] One skilled in the art would understand that devices within a family of devices can have different footprints (i.e., footprint variations). For example, the specification states:

> Devices with combined programmable logic and high-speed serial channels are increasingly appearing in the marketplace. However, **defining unique pinouts for parts** with different programmable density or different high-speed serial transmission bandwidth **within a family of parts** makes applicability difficult for users (i.e., migration between higher and lower density parts). For example, **when a user desires to switch to a transceiver with a larger number of high-speed serial channels**, the board layout for the transceiver chip needs to be changed. Such **a change can include the footprint of the transceiver device**, routing of the transceiver chip, and/or other affected routing on the board. Additionally, complex routing and timing issues between the devices will have to be resolved (page 2, lines 3-15 of the specification, emphasis added).

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[19] See entry for variation from Merriam-Webster Online Thesaurus attached as Exhibit A in the Appendix.

[20] See examples of the art-recognized meaning of the term footprint attached as Exhibit B in the Appendix.

With respect to the relationship between the steps of claim 1, step (A) recites defining a pinlist. The step (B) of claim 1 recites generating a superset listing of pins from the pinlist defined in the step (A). The step (C) of claim 1 recites creating the superset pinout from the superset listing of pins generated in the step (B). Thus, one of ordinary skill in the art would clearly understand the relationship between the steps of claim 1 based on the plain meaning of the claim language.

Furthermore, with respect to the relationship between generating the superset pinout and eliminating footprint variations, the specification states:

> While in the state 52, the process 50 may **define the pinlist for each device within a family of devices**. The process 50 may define what pins and how many of each are required for each device (**as if generating a unique pinout for that device**). For example, if there are two members in the family for which to create a superset pinout, then the individual pinlist may be:
>
> MEMBERA: AABC (two pins of A)
> MEMBERB: ABD
>
> While in the state 54, the process 50 may generate a superset listing of pins from the individual pinlist (e.g., combining pins that can be shared by more than one member). The process 50 may note which pins are applicable to which device members. Therefore, from the two members MEMBERA and MEMBERB, the superset pinlist may be AABCD (page 6, line 17 through page 7, line 11 of the specification, emphasis added).

The specification further states:

> The present invention may be directed to **a method for generating superset pinout for devices** with combined programmable logic with high-speed serial channels. **The method** 50 (or 50') **may provide common footprints and layouts for a family of devices** (page 6, lines 10-13 of the specification, emphasis added).

One skilled in the art would clearly understand that creating a superset pinout (e.g., five pins AABCD) that provides a common footprint for each member of a family of devices relates to

eliminating footprint variations (e.g., four pins AABC for member A and three pins ABD for member B if unique pinouts are implemented) within the family of devices. Thus, one of ordinary skill in the pertinent art reading the presently pending claims in light of the specification would be reasonably apprised of the meets and bounds of the presently claimed invention. Therefore, the Examiner failed to meet the Office's burden of factually supporting a *prima facie* conclusion that the present claims are not definite. As such, the presently pending claims of group 1 are fully patentable under the second prong of 35 U.S.C. §112, second paragraph, and the rejection should be reversed.

Furthermore, the Examiner's conclusory statement that "footprint variations cannot be eliminated where there is first no prior recitation of their creation"[21] does not adequately explain why the scope of the claims would not be clear to **a person possessing the ordinary level of skill in the pertinent art when read in light of the specification.**[22] Specifically, the Examiner fails to clearly state whether the prior recitation she is looking for should appear in (i) the preamble, (ii) the specification or (iii) the other claim elements. The mere fact that the body of a claim recites additional elements which do not appear in the claim's preamble does not render the claim indefinite under 35 U.S.C.112, second paragraph.[23] Furthermore, The mere fact that a term or phrase used in

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[21] See page 3, lines 3-4 of the final Office Action dated December 30, 2003 and page 2, section no. 3, lines 6-7 of the Advisory Action dated March 22, 2004.

[22] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003.

[23] MPEP § 2173.05(e), citing *In re Larsen*, No.01-1092 (Fed. Cir. May 9, 2001) (unpublished) (The preamble of the *Larsen* claim recited only a hanger and a loop but the body of the claim positively recited a linear member. The examiner rejected the claim under 35 U.S.C.112, second paragraph, because the omission from the claim 's preamble of a critical element (i.e., a linear member) renders that claim indefinite. The court reversed the examiner 's rejection and stated that the totality of all the limitations of the claim and their interaction with each other must be considered

the claims has no antecedent basis in the specification disclosure does not mean, necessarily, that the term or phrase is indefinite.[24] There is no requirement that the words in the claims must match those used in the specification disclosure.[25] The MPEP states:

> The Examiner's task of making sure the claim language complies with the requirements of the statute should be carried out in a positive and constructive way, so that minor problems can be identified and easily corrected, and so that the major effort is expended on more substantive issues.[26]

With respect to carrying out the Examiner's task, the MPEP provides that the Examiner should "suggest corrections to antecedent problems."[27] Furthermore, the MPEP states:

> In reviewing a claim for compliance with 35 U.S.C. 112, second paragraph, the examiner must consider the claim as a whole to determine whether the claim apprises one of ordinary skill in the art of its scope and, therefore, serves the notice function required by 35 U.S.C.112, second paragraph, by providing clear warning to others as to what constitutes infringement of the patent. See, e.g., *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1379, 55 USPQ2d 1279, 1283 (Fed. Cir. 2000). If the language used by Applicant satisfies the statutory requirements of 35 U.S.C. 112, second paragraph, but the Examiner merely wants the Applicant to improve the clarity or precision of the language used, the claim must not be rejected under 35 U.S.C.112, second paragraph, rather, **the examiner should suggest improved language to the Applicant**.[28]

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to ascertain the inventor 's contribution to the art. Upon review of the claim in its entirety, the court concluded that the claim at issue apprises one of ordinary skill in the art of its scope and, therefore, serves the notice function required by 35 U.S.C.112, paragraph 2.).

[24] MPEP § 2173.05.

[25] *Id.*

[26] MPEP § 2173.05(e) EXAMINER SHOULD SUGGEST CORRECTION TO ANTECEDENT PROBLEMS.

[27] *Id.*

[28] MPEP §2173.02, emphasis added.

Contrary to the Patent Office's policy as expressed in the MPEP, the Examiner has refused numerous invitation by Appellant's representatives to suggest corrections that would be acceptable.

Furthermore, the Appellant's representative has made an extensive effort to provide claim language to which the Examiner will not object. However, the Examiner appears to want Appellants to keep guessing at what language will ultimately be acceptable. Specifically, Appellant's representative spent two hours in a telephone interview with the Examiner trying to resolve the rejection.[29] Appellant's representative followed up the two hour telephone interview by submitting a proposed amendment containing language which was believed to have been agreed to by the Examiner.[30] The Examiner's response was a cryptic reply that "the response does not place this application in a condition for allowance."[31] When Appellant's representative asked the Examiner to clarify whether the amendment was what had been agreed to, the Examiner again cryptically replied "Partially. There is still more work to be done."[32] An Amendment After Final was filed on March 22, 2004 which included amendments that Appellants believed would overcome the § 112 rejection. The Amendment After Final was entered, however, the Examiner maintained the § 112 rejections.[33] Although Appellant's representatives made further attempts to determine what the Examiner was seeking, the Examiner refused to discuss any further what language she

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[29] See Interview Summary dated March 8, 2004 (paper no. 6).

[30] See e-mail message dated February 26, 2004, attached as Exhibit C in the Appendix.

[31] See e-mail message dated February 27, 2004, attached as Exhibit D in the Appendix.

[32] See e-mail message dated February 27, 2004, attached as Exhibit E in the Appendix.

[33] See Advisory Action dated May 12, 2004 (paper no. 050604).

would find acceptable. The Examiner's responses clearly were not suggestions for corrections or improved language as encouraged by the MPEP.

In yet another effort to materially advance the prosecution of the application, Appellant's representatives took the extraordinary step of asking the Examiner's supervisor whether he could suggest a correction or improved language in light of the Examiner's statements. The Examiner's supervisor stated that in his view, the addendum to the Advisory Action[34] provided:

> . . . a roadmap on what needed to be done to the claims and what areas needed to be addressed.[35]

The Examiner's supervisor further stated:

> . . . an earlier reference in the claims was needed to provide "structural connection" for layout variations or footprint variation.[36]

Although Appellant's representative did not necessarily agree with the solution proposed by the Examiner's supervisor, in a last attempt to materially advance the prosecution of the application to allowance, a second Amendment After Final was filed on May 27, 2004 in which an earlier reference in the claim 1 was made for footprint variations. Specifically, the currently pending claim 1 reads as follows:

> 1. A method for generating a superset pinout for a family of devices, comprising the steps of:
> (A) defining a pinlist for each device within said family of devices;
> (B) generating a superset listing of pins from said pinlist;
> (C) creating said superset pinout for said family of devices from said superset listing of pins to eliminate potential footprint variations

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[34] Dated May 12, 2004 (paper no. 050604).

[35] See Inteview Summary dated May 25, 2004 (paper no. 05202004).

[36] *Id.*

within said family of devices; and
(D) marking each pin of said superset pinout associated with each member of said family of devices.

The amended claim 1 submitted in the Amendment After Final filed May 27, 2004 read as follows:

1. (CURRENTLY AMENDED) A method for generating a superset pinout for a family of devices having potential footprint variations, comprising the steps of:
(A) defining a pinlist for each device within said family of devices;
(B) generating a superset listing of pins from said pinlist;
(C) creating said superset pinout for said family of devices from said superset listing of pins to eliminate said potential footprint variations within said family of devices; and
(D) marking each pin of said superset pinout associated with each member of said family of devices.

In an Advisory Action, the Examiner stated that the Amendment After Final[37] would not be entered because the added limitation of "having footprint variations" in the independent claims would narrow the scope of the claims and, therefore, require further consideration and/or search.[38] However, the file history is clear that extensive consideration has already been given. In particular, the Examiner presumably performed a thorough search[39] with respect to "footprint variations" and "layout variations."[40] Specifically, claim 5 as originally filed recited:

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[37] Filed May 27, 2004.

[38] See page 2 of the Advisory Action dated July 12, 2004 (paper no. 070804).

[39] See 37 CFR1.104(a)(1); (On taking up an application for examination . . the examiner shall make a thorough study thereof and shall make a thorough investigation of the available prior art relating to the subject matter of the claimed invention . . . .).

[40] See page 5, Allowable Subject Matter, in the Office Action dated July 14, 2003 (paper no. 3).

> 5. The method according to claim 1, wherein step (C) further comprises:
>
> eliminating **footprint variations** within said family of devices with said superset pinout.

Claim 6 as originally presented recited:

> 6. The method according to claim 1, wherein step (C) further comprises:
>
> eliminating **layout variations** within said family of devices with said superset pinout.

The Examiner stated that the originally presented claims 5 and 6 contained allowable subject matter.[41] The Examiner has already considered and/or searched footprint and layout variations and found them allowable over the art of record. It is Appellant's understanding that the Examiner would not indicate particular claims are allowable without sufficient consideration and/or search.

Contrary to the position taken by the Examiner, one skilled in the art would be able to ascertain the meaning of the phrase "to eliminate potential footprint variations within the family of devices" in light of the specification. The test for definiteness under 35 U.S.C.112, second paragraph, is whether "those skilled in the art would understand what is claimed when the claim is read in light of the specification."[42] If one skilled in the art is able to ascertain the meaning of the phrase "to eliminate potential footprint variations within the family of devices" in light of the specification, 35 U.S.C.112, second paragraph, is satisfied.[43] Despite the position taken by the Examiner, one skilled in the art would be able to ascertain the meaning of the phrase "to eliminate

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[41] See page 5, Allowable Subject Matter, in the Office Action dated July 14, 2003 (paper no. 3).

[42] *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 USPQ2d 1081, 1088 (Fed. Cir. 1986).

[43] MPEP § 2173.02.

potential footprint variations within the family of devices" in light of the specification. As such, the claims of group 1 are fully patentable under 35 U.S.C. § 112, second paragraph, and the rejection should be reversed.

Specifically, one **skilled** in the art would understand that the existence of footprint variations is implied by a step involving elimination of the footprint variations. Therefore, a separate recitation of their existence or creation is not necessary. Furthermore, one skilled in the art would further recognize that footprint variations may be eliminated by preventing their creation to begin with. Thus, requiring that the claims include a recitation of the creation of footprint variations would not result in a clear and distinct claiming of the invention. Furthermore, one skilled in the art would be able to ascertain the meaning of the phrase "to eliminate potential footprint variations within the family of devices" in light of the specification. The specification includes two drawings (e.g., FIGS. 2 and 3) which show example layouts (or footprints) for different members of a family of devices.[44] Furthermore, the specification states:

> **Transceiver devices (or the like) with varying number of channels have unique pinouts to accommodate the varying I/O requirements.** However, increasing the number of pins increases power consumption. Larger numbers of channels also need additional die space. Furthermore, **programmable logic devices (PLDs) and transceiver devices are typically mounted in separate packages to accommodate unique I/O packaging requirements for each device** (page 1, line 14 through page 2, line 2 of the specification).

The specification further states:

> Devices with combined programmable logic and high-speed serial channels are increasingly appearing in the marketplace. However,

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[44] See the description of FIGS. 2 and 3 on page 9, line 4 through page 10, line 6 of the specification.

> **defining unique pinouts for parts** with different programmable density or different high-speed serial transmission bandwidth **within a family of parts** makes applicability difficult for users (i.e., migration between higher and lower density parts). For example, **when a user desires to switch to a transceiver** with a larger number of high-speed serial channels, **the board layout for the transceiver chip needs to be changed. Such a change can include the footprint of the transceiver device**, routing of the transceiver chip, and/or other affected routing on the board. Additionally, complex routing and timing issues between the devices will have to be resolved (page 2, lines 3-15 of the specification).

Thus, in light of the specification, one skilled in the art would recognize that devices within a family of devices can have unique footprints (e.g., footprint variations).

One skilled in the art would also be able, in light of the specification, to ascertain the meaning of "to eliminate footprint variations within a family of devices." In particular, the specification provides the following example:

> The process 50 (or 50') may **eliminate footprint changes** when users replace a device with another having a different programmable logic gate density while **in the same family, since a common footprint exists for the two members**. The process 50 may eliminate footprint changes when users replace a device with another having a different number of high-speed serial channels while in the same family, since a common footprint exists for the two members (page 10, line 14 through page 11, line 2 of the specification, emphasis added).

Other examples provided by the specification include:

> The process 50 (or 50') may allow migration from one member to another member to **not involve changes in footprint** or layout (page 5, lines 17-19 of the specification, emphasis added).
>
> The method 50 (or 50') may **provide common footprints** and layouts **for a family of devices** (page 6, lines 12-13 of the specification, emphasis added).
>
> Therefore, the process 50 may **provide a footprint that may be common to all members in the family** and a superset pinout that

accommodates the needs of all members (page 8, lines 13-16 of the specification, emphasis added).

In one example, the circuit 100' may be another PSI family member with 100K programmable logic gate density and two sets of transceiver channels at 2.5Gbps. The circuit 100' may be InfiniBand compliant (e.g., a serial transceiver function). In another example, the circuit 100' may **have the same footprint** and layout, for another member with different locations of no-connect pins and the transceiver being SONET compliant (page 9, line 19 through page 10, line 6 of the specification, emphasis added).

The process 50 (or 50') may generate a superset pinout for a family of programmable serial interface (PSI) devices. The process 50 (or 50') may allow for different gate densities and different numbers and functions of transceiver channels to be accommodated by a superset pinout. The process 50 (or 50') may provide a user with a PSI device design migration path to higher CPLD gate densities and more SERDES transceiver bandwidth within a common footprint. The process 50 (or 50') **may eliminate footprint changes** when users replace a device with another having a different programmable logic gate density while in the same family, since a common footprint exists for the two members. The process 50 may **eliminate footprint changes** when users replace a device with another having a different number of high-speed serial channels **while in the same family**, since **a common footprint exists for the two members** (page 10, line 7 through page 11, line 2 of the specification, emphasis added).

The process 50 (or 50') may **eliminate footprint changes** and reduce or eliminate layout changes when users replace a device with another having different functions for the high-speed serial channels. The process 50 (or 50') may reduce or eliminate routing changes when users replace a device with another having a different programmable logic gate density while in the same family, since **a common footprint exists for the two members**. Therefore, users may design board layouts to accommodate for more than one member of a family without external components to allow for later changes, without affecting layout. The process 50 (or 50') may reduce or eliminate layout changes when users replace a device with another having a different number of high-speed serial channels while in the same family(page 11, lines 3-15 of the specification, emphasis added).

The process 50 (or 50') may provide additional cost savings for manufacturers. For example, one device member having one serial

> channel may call for a single transceiver block. **At the same time, another member in the same family may have the same footprint** and two transceivers channels (e.g., implement two transceivers blocks). The method 50 (or 50') may allow the devices to have the same layout, while the device having fewer channels may not incur the additional cost of a second transceiver block (page 11, line 16 through page 12, line 4 of the specification, emphasis added).

For the reasons presented above, one of ordinary skill in the pertinent art reading the presently pending claims in light of the specification would be able to reasonably ascertain the meets and bounds of the presently claimed invention. As such, the claims of group 1 are fully patentable under 35 U.S.C. §112, second paragraph and the rejection should be reversed.

2. Group 2 (claim 10) is fully patentable under 35 U.S.C. § 112, second paragraph.

Claim 10 depends directly from claim 1 and, therefore, includes all the limitations of claim 1. As such, the arguments present in support of claim 1 are hereby incorporated by reference in support of claim 10. Claim 10 further recites that step (C) further comprises designing a board layout (i) to accommodate more than one member of the family of devices and (ii) to allow for late changes without affecting the board layout and without external components.

The recitation in claim 10 of "designing a board layout (i) to accommodate more than one member of the family of devices and (ii) to allow for late changes without affecting the board layout and without external components" meets the objective test of defining the metes and bounds of the subject matter by reciting what the superset pinout created by the means for creating does. The Examiner's conclusory statement that claim 10 "is unclear as to what late changes will be

allowed; furthermore 'without external components' is a dangling phrase and seem [sic] unrelated to the rest of the claim,"[45] does not provide any analysis of why the scope of claim 10 would not be clear to **a person possessing the ordinary level of skill in the pertinent art when read in light of the specification.**[46] In rejecting a claim under the second paragraph of 35 U.S.C. §112, it is incumbent on the Examiner to establish that one of ordinary skill in the pertinent art, when reading the claims **in light of the supporting specification**, would not have been able to ascertain with a reasonable degree of precision and particularity the particular area set out and circumscribed by the claims.[47] Since the Examiner has not presented an analysis of why one of ordinary skill in the pertinent art, when reading the claims **in light of the supporting specification**, would not have been able to ascertain with a reasonable degree of precision and particularity the particular area set out and circumscribed by the claims, the Examiner has not met the Office's burden to establish that one of ordinary skill in the pertinent art, when reading the claims in light of the supporting specification, would not have been able to ascertain with a reasonable degree of precision and particularity the particular area set out and circumscribed by the claims.[48] As such, claim 10 is patentable under 35 U.S.C. § 112, second paragraph and the rejection should be reversed.

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[45] See paragraph no. 4 on page 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604).

[46] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604). See also MPEP § 2173.02.

[47] *Ex parte Wu*, 10 USPQ2d 2031, 2033 (B.P.A.I. 1989) (citing *In re Moore*, 439 F.2d 1232, 169 USPQ 236 (C.C.P.A. 1971); *In re Hammack*, 427 F.2d 1378, 166 USPQ 204 (C.C.P.A. 1970)).

[48] *Ex parte Wu*, 10 USPQ2d 2031, 2033 (B.P.A.I. 1989) (citing *In re Moore*, 439 F.2d 1232, 169 USPQ 236 (C.C.P.A. 1971); *In re Hammack*, 427 F.2d 1378, 166 USPQ 204 (C.C.P.A. 1970)).

Furthermore, one of ordinary skill in the pertinent art, when reading claim 10 **in light of the supporting specification**, would have been able to ascertain with a reasonable degree of precision and particularity the particular area set out and circumscribed. In particular, the specification states:

> The process 50 (or 50') may eliminate footprint changes and reduce or eliminate layout changes when users replace a device with another having different functions for the high-speed serial channels. The process 50 (or 50') may reduce or eliminate routing changes when users replace a device with another having a different programmable logic gate density while in the same family, since a common footprint exists for the two members. **Therefore, users may design board layouts to accommodate for more than one member of a family without external components to allow for later changes, without affecting layout**. The process 50 (or 50') may reduce or eliminate layout changes when users replace a device with another having a different number of high-speed serial channels while in the same family (page 11, lines 3-15 of the specification, emphasis added).

For the reasons presented above, one of ordinary skill in the pertinent art reading the presently pending claim 10 in light of the specification would be able to reasonably ascertain the meets and bounds of the presently claimed invention. As such, claim 10 is fully patentable under 35 U.S.C. §112, second paragraph and the rejection should be reversed.

3. Group 3 (claim 19) is fully patentable under 35 U.S.C. § 112, second paragraph.

The presently pending claim 19 provides an apparatus for generating a superset pinout for a family of devices comprising: (i) means for defining a pinlist for each device within the family of devices, (ii) means for generating a superset listing of pins from the pinlist, (iii) means for creating the superset pinout for the family of devices from the superset listing of pins, where the superset

pinout eliminates layout variations within the family of devices and (iv) means for marking each pin of the superset pinout associated with each member of the family of devices.

The Examiner failed to explicitly state whether the rejection of claim 19 under 35 U.S.C. §112, second paragraph, is based on the failure to claim what the Appellants regard as their invention or on indefiniteness.[49] Therefore, both prongs are addressed for completeness. Whether the claims set forth the subject matter regarded by the Appellants as their invention is a subjective test that is satisfied as evidenced by the submission of claim 19 for examination. The Examiner failed to present any evidence or convincing line of reasoning to support a conclusion that the invention set forth in claim 19 is not what the Appellants regard as their invention.[50] The invention set forth in the claims **must be presumed, in the absence of evidence to the contrary, to be that which Appellants regard as their invention.**[51] Since the Examiner presented no evidence or convincing line of reasoning to doubt the invention set forth in claim 19 is what the Appellants regard as their invention, the presumption that the claims are directed to that which the Applicants regard as their invention is intact. As such, claim 19 is patentable under the first prong of 35 U.S.C. §112, second paragraph, and the rejection should be reversed.

With regard to the second requirement above, the recitation in claim 19 of "the superset pinout eliminates layout variations within the family of devices" meets the objective test

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[49] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604).

[50] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604).

[51] MPEP §2172(I), citing *In re Moore*, 439 F.2d 1232, 169 USPQ 236 (C.C.P.A. 1971).

of defining the metes and bounds of the subject matter by reciting what the superset pinout created by the means for creating does. The Examiner's conclusory statement that claim 19 is "incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections" where the "omitted structural cooperative relationship" is "the relation between *layout variations* and the rest of the claim,"[52] does not provide any analysis of why the scope of claim 19 would not be clear to **a person possessing the ordinary level of skill in the pertinent art when read in light of the specification**.[53] In rejecting a claim under the second paragraph of 35 U.S.C. §112, it is incumbent on the Examiner to establish that one of ordinary skill in the pertinent art, when reading the claims in light of the supporting specification, would not have been able to ascertain with a reasonable degree of precision and particularity the particular area set out and circumscribed by the claims.[54] The Examiner has not met the Office's burden to establish that one of ordinary skill in the pertinent art, when reading the claims in light of the supporting specification, would not have been able to ascertain with a reasonable degree of precision and particularity the particular area set out and circumscribed by the claims.[55] As such, claim 19 is patentable under 35 U.S.C. § 112, second paragraph and the rejection should be reversed.

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[52] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604).

[53] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604). See also MPEP § 2173.02.

[54] *Ex parte Wu*, 10 USPQ2d 2031, 2033 (B.P.A.I. 1989) (citing *In re Moore*, 439 F.2d 1232, 169 USPQ 236 (C.C.P.A. 1971); *In re Hammack*, 427 F.2d 1378, 166 USPQ 204 (C.C.P.A. 1970)).

[55] *Ex parte Wu*, 10 USPQ2d 2031, 2033 (B.P.A.I. 1989) (citing *In re Moore*, 439 F.2d 1232, 169 USPQ 236 (C.C.P.A. 1971); *In re Hammack*, 427 F.2d 1378, 166 USPQ 204 (C.C.P.A. 1970)).

The statement by the Examiner that the claims are "incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections"[56] clearly does not adequately address, *inter alia*, (i) what is considered to be the pertinent art, (ii) what the level of skill is in the pertinent art and (iii) why **one of ordinary skill in the pertinent art, when reading the claims in light of the specification, would not have been able to reasonably ascertain the specific area set out and circumscribed by the claims**. It is not essential to a patentable combination that there be interdependency between the elements of the claimed device or that all the elements operate concurrently toward the desired result.[57] Furthermore, a claim does not necessarily fail to comply with 35 U.S.C. §112, second paragraph where the various elements do not function simultaneously, are not directly functionally related, do not directly intercooperate, and/or serve independent purposes.[58] Therefore, the Examiner failed to meet the Office's burden of factually supporting a *prima facie* conclusion that the present claims are not definite. As such, the presently pending claim 19 is fully patentable under the second prong of 35 U.S.C. §112, second paragraph, and the rejection should be reversed.

Furthermore, one of ordinary skill in the art when reading the claims in light of the specification would clearly understand the relationship between the elements of claim 19. Specifically, the meaning of the terms used in the claim is clearly apparent from the prior art or from the specification and drawings as originally filed. In particular, variations would be understood to

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[56] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003.

[57] MPEP § 2171.01, citing *Ex parte Nolden*, 149 USPQ 378, 380 (Bd. Pat. App.1965).

[58] MPEP § 2171.01, citing *Ex parte Huber,* 148 USPQ 447, 448-49 (Bd. Pat. App. 1965).

refer to changes, differences, dissimilarities, etc.[59] With respect to the terms "pinout" and "pinlist," the specification states:

> **Pinout** may refer to a layout of the signals for a device (e.g., a list of physical pins of a device package and functions assigned to those pins). For example, a pinout may be a list of pins and pin functions for quad flat pack (QFP) (e.g., pin1 = ground, pin2 = signal A, etc.) and for a ball grid array (BGA) (e.g., A1=Ground, A2 = signal A, etc.) **Pinlist** may refer to a list of signals for a device to be assigned to physical pins to become the functions of the pins (e.g., the ground, signal A, etc.). For simplicity a BGA ball may also be referred to as a pin (page 6, lines 1-9 of the specification, emphasis added).

With respect to the term "layout," one of ordinary skill in the art would recognize the term "layout", with respect to a device, to refer to the physical pinout or pattern of connections to pins (or balls) of the device.[60] One skilled in the art would understand that devices within a family of devices can have different footprints and, therefore, different layouts. For example, the specification states:

> Devices with combined programmable logic and high-speed serial channels are increasingly appearing in the marketplace. However, **defining unique pinouts for parts** with different programmable density or different high-speed serial transmission bandwidth **within a family of parts** makes applicability difficult for users (i.e., migration between higher and lower density parts). For example, when a user desires to switch to a transceiver with a larger number of high-speed serial channels, **the board layout for the transceiver chip needs to be changed. Such a change can include the footprint of the transceiver device, routing of the transceiver chip, and/or other affected routing on the board.** Additionally, complex routing and timing issues between the devices will have to be resolved (page 2, lines 3-15 of the specification, emphasis added).

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[59] See entry for variation from Merriam-Webster Online Thesaurus attached in the Appendix as Exhibit A.

[60] See Exhibit B in the Appendix for examples of layouts for various footprints.

With respect to the relationship between the elements of claim 19, claim 19 recites (i) means for defining A PINLIST for each device within the family of devices, (ii) means for generating A SUPERSET LISTING OF PINS **from** THE PINLIST, (iii) means for creating THE SUPERSET PINOUT FOR THE FAMILY OF DEVICES **from** THE SUPERSET LISTING OF PINS, where the superset pinout eliminates layout variations within the family of devices. Thus, one of ordinary skill in the art would clearly understand the relationship between the elements of claim 19 based on the claim language.

Furthermore, with respect to the relationship between the superset pinout and eliminating layout variations, the specification provides an example:

> While in the state 52, the process 50 may **define the pinlist for each device within a family of devices**. The process 50 may define what pins and how many of each are required for each device (**as if generating a unique pinout for that device**). For example, if there are two members in the family for which to create a superset pinout, then the individual pinlist may be:
>
> MEMBERA: AABC (two pins of A)
> MEMBERB: ABD
>
> While in the state 54, the process 50 may generate a superset listing of pins from the individual pinlist (e.g., combining pins that can be shared by more than one member). The process 50 may note which pins are applicable to which device members. Therefore, from the two members MEMBERA and MEMBERB, the superset pinlist may be AABCD (page 6, line 17 through page 7, line 11 of the specification, emphasis added).

The specification further states:

> The present invention may be directed to a method for **generating superset pinout for devices** with combined programmable logic with high-speed serial channels. The method 50 (or 50') **may provide common footprints and layouts for a family of devices** (page 6, lines 10-13 of the specification, emphasis added).

One skilled in the art would clearly understand that creating a superset pinout (e.g., five pins AABCD) that provides common footprints and **layouts** for each member of a family of devices relates to eliminating layout variations (e.g., four pins AABC for member A and three pins ABD for member B if unique pinouts are implemented) within the family of devices. Thus, one of ordinary skill in the pertinent art reading the presently pending claims in light of the specification would be reasonably apprised of the meets and bounds of the presently claimed invention. Therefore, the Examiner failed to meet the Office's burden of factually supporting a *prima facie* conclusion that the present claims are not definite. As such, the presently pending claim 19 is fully patentable under the second prong of 35 U.S.C. §112, second paragraph, and the rejection should be reversed.

Furthermore, the Examiner's conclusory statement that "layout variations cannot be eliminated where there is first no prior recitation of their creation."[61] does not adequately explain why the scope of the claims would not be clear to **a person possessing the ordinary level of skill in the pertinent art when read in light of the specification.**[62] Specifically, the Examiner fails to clearly state whether the prior recitation she is looking for should appear in (i) the preamble, (ii) the specification or (iii) the other claim elements. The mere fact that the body of a claim recites additional elements which do not appear in the claim's preamble does not render the claim indefinite under 35 U.S.C.112, second paragraph.[63] Furthermore, The mere fact that a term or phrase used in

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[61] See page 3, lines 3-4 of the final Office Action dated December 30, 2003 and page 2, section no. 3, lines 6-7 of the Advisory Action dated March 22, 2004.

[62] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003.

[63] MPEP § 2173.05(e), citing *In re Larsen*, No.01-1092 (Fed. Cir. May 9, 2001) (unpublished) (The preamble of the *Larsen* claim recited only a hanger and a loop but the body of the claim positively recited a linear member. The examiner rejected the claim under 35 U.S.C.112, second paragraph, because the omission from the claim 's preamble of a critical element (i.e., a linear

the claims has no antecedent basis in the specification disclosure does not mean, necessarily, that the term or phrase is indefinite.[64] There is no requirement that the words in the claims must match those used in the specification disclosure.[65] The MPEP states:

> The Examiner's task of making sure the claim language complies with the requirements of the statute should be carried out in a positive and constructive way, so that minor problems can be identified and easily corrected, and so that the major effort is expended on more substantive issues.[66]

With respect to carrying out the Examiner's task, the MPEP provides that the Examiner should "suggest corrections to antecedent problems."[67] Furthermore, the MPEP states:

> In reviewing a claim for compliance with 35 U.S.C. 112, second paragraph, the examiner must consider the claim as a whole to determine whether the claim apprises one of ordinary skill in the art of its scope and, therefore, serves the notice function required by 35 U.S.C.112, second paragraph, by providing clear warning to others as to what constitutes infringement of the patent. See, e.g., *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1379, 55 USPQ2d 1279, 1283 (Fed. Cir. 2000). If the language used by Applicant satisfies the statutory requirements of 35 U.S.C. 112, second paragraph, but the Examiner merely wants the Applicant to improve the clarity or precision of the language used, the claim must not be rejected under

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member) renders that claim indefinite. The court reversed the examiner 's rejection and stated that the totality of all the limitations of the claim and their interaction with each other must be considered to ascertain the inventor 's contribution to the art. Upon review of the claim in its entirety, the court concluded that the claim at issue apprises one of ordinary skill in the art of its scope and, therefore, serves the notice function required by 35 U.S.C.112, paragraph 2.).

[64] MPEP § 2173.05.

[65] *Id.*

[66] MPEP § 2173.05(e) EXAMINER SHOULD SUGGEST CORRECTION TO ANTECEDENT PROBLEMS.

[67] *Id.*

> 35 U.S.C.112, second paragraph, rather, **the examiner should suggest improved language to the Applicant.**[68]

Contrary to the Patent Office's policy as expressed in the MPEP, the Examiner has refused numerous invitation by Appellant's representatives to suggest corrections that would be acceptable.

Furthermore, the Appellant's representative has made an extensive effort to provide claim language to which the Examiner will not object. However, the Examiner appears to want Appellant to keep guessing at what language will ultimately be acceptable. Specifically, Appellant's representative spent two hours in a telephone interview with the Examiner trying to resolve the rejection.[69] Appellant's representative followed up the two hour telephone interview by submitting a proposed amendment containing language which was believed to have been agreed to by the Examiner.[70] The Examiner's response was a cryptic reply that "the response does not place this application in a condition for allowance."[71] When Appellant's representative asked the Examiner to clarify whether the amendment was what had been agreed to, the Examiner again cryptically replied "Partially. There is still more work to be done."[72] An Amendment After Final was filed on March 22, 2004 which included amendments that Appellant believed would overcome the § 112 rejection. The Amendment After Final was entered, however, the Examiner maintained the § 112 rejections.[73] Although Appellant's representatives made further attempts to determine what the

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[68] MPEP §2173.02, emphasis added.

[69] See Interview Summary dated March 8, 2004 (paper no. 6).

[70] See e-mail message dated February 26, 2004, attached as Exhibit C in the Appendix.

[71] See e-mail message dated February 27, 2004, attached as Exhibit D in the Appendix.

[72] See e-mail message dated February 27, 2004, attached as Exhibit E in the Appendix.

[73] See Advisory Action dated May 12, 2004 (paper no. 050604).

Examiner was seeking, the Examiner refused to discuss any further what language she would find acceptable. The Examiner's responses clearly were not suggestions for corrections or improved language as encouraged by the MPEP.

In yet another effort to materially advance the prosecution of the application, Appellant's representatives took the extraordinary step of asking the Examiner's supervisor whether he could suggest a correction or improved language in light of the Examiner's statements. The Examiner's supervisor stated:

> . . . an earlier reference in the claims was needed to provide "structural connection" for layout variations or footprint variation.[74]

Although Appellant's representative did not necessarily agree with the solution proposed by the Examiner's supervisor, in a last attempt to materially advance the prosecution of the application to allowance, a second Amendment After Final was filed on May 27, 2004 in which an earlier reference in the claim 19 was made for footprint variations. Specifically, the currently pending claim 19 reads as follows:

> 19. An apparatus for generating a superset pinout for a family of devices comprising:
> means for defining a pinlist for each device within said family of devices;
> means for generating a superset listing of pins from said pinlist;
> means for creating said superset pinout for said family of devices from said superset listing of pins, wherein said superset pinout eliminates layout variations within said family of devices; and
> means for marking each pin of said superset pinout associated with each member of said family of devices.

The amended claim 19 submitted in the Amendment After Final filed May 27, 2004 read as follows:

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[74] *Id.*

> 19. (CURRENTLY AMENDED) An apparatus for generating a superset pinout for a family of devices having layout variations comprising:
>
> means for defining a pinlist for each device within said family of devices;
>
> means for generating a superset listing of pins from said pinlist;
>
> means for creating said superset pinout for said family of devices from said superset listing of pins, wherein said superset pinout eliminates said layout variations within said family of devices; and
>
> means for marking each pin of said superset pinout associated with each member of said family of devices.

In an Advisory Action, the Examiner stated that the Amendment After Final[75] would not be entered because:

> the added limitation, "having footprint variations" in the independent claims, narrows the scope of the claims. Therefore, further consideration and/or search is required..[76]

However, the file history is clear that extensive consideration has already been given. In particular, the Examiner presumably performed a thorough search[77] with respect to "footprint variations" and "layout variations."[78] Specifically, claim 5 as originally filed recited:

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[75] Filed May 27, 2004.

[76] See page 2 of the Advisory Action dated July 12, 2004 (paper no. 070804).

[77] See 37 CFR1.104(a)(1); (On taking up an application for examination . . the examiner shall make a thorough study thereof and shall make a thorough investigation of the available prior art relating to the subject matter of the claimed invention . . . .).

[78] See page 5, Allowable Subject Matter, in the Office Action dated July 14, 2003 (paper no. 3).

> 5. The method according to claim 1, wherein step (C) further comprises:
>
> eliminating **footprint variations** within said family of devices with said superset pinout.

Claim 6 as originally presented recited:

> 6. The method according to claim 1, wherein step (C) further comprises:
>
> eliminating **layout variations** within said family of devices with said superset pinout.

The Examiner stated that the originally presented claims 5 and 6 contained allowable subject matter.[79] The Examiner has already considered and/or searched footprint and layout variations and found them allowable over the art of record. It is Appellant's understanding that the Examiner would not indicate particular claims are allowable without sufficient consideration and/or search. Furthermore, the Examiner's remark fails to fully address the specific added phrase "having layout variations." Furthermore, the Examiner failed to address whether the added phrase provided the earlier reference which the Examiner had asserted was needed.

Contrary to the position taken by the Examiner, one skilled in the art would be able to ascertain the meaning of the phrase "where the superset pinout eliminates layout variations within the family of devices" in light of the specification. The test for definiteness under 35 U.S.C. §112, second paragraph, is whether "those skilled in the art would understand what is claimed when the claim is read in light of the specification."[80] If one skilled in the art is able to ascertain the meaning of the phrase "to eliminate potential footprint variations within the family of devices" in light of the

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[79] See page 5, Allowable Subject Matter, in the Office Action dated July 14, 2003 (paper no. 3).

[80] *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 USPQ2d 1081, 1088 (Fed. Cir. 1986).

specification, 35 U.S.C. §112, second paragraph, is satisfied.[81] Despite the position taken by the Examiner, one skilled in the art would be able to ascertain the meaning of the phrase "where the superset pinout eliminates layout variations within the family of devices" in light of the specification. As such, claim 19 is fully patentable under 35 U.S.C. § 112, second paragraph, and the rejection should be reversed.

Specifically, one **skilled** in the art would understand that the existence of layout variations is implied by the statement that the superset pinout eliminates layout variations. Therefore, a separate recitation of their existence or creation is not necessary. Furthermore, one skilled in the art would further recognize that layout variations may be eliminated by preventing their creation to begin with. Thus, requiring that the claims include a recitation of the creation of layout variations would not result in a clear and distinct claiming of the invention. Furthermore, one skilled in the art would be able to ascertain the meaning of the phrase "the superset pinout eliminates layout variations within the family of devices" in light of the specification. The specification includes two drawings (e.g., FIGS. 2 and 3) which show example layouts for different members of a family of devices.[82] Furthermore, the specification states:

> **Transceiver devices (or the like) with varying number of channels have unique pinouts to accommodate the varying I/O requirements.** However, increasing the number of pins increases power consumption. Larger numbers of channels also need additional die space. Furthermore, **programmable logic devices (PLDs) and transceiver devices are typically mounted in separate packages to accommodate unique I/O packaging requirements**

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[81] MPEP § 2173.02.

[82] See the description of FIGS. 2 and 3 on page 9, line 4 through page 10, line 6 of the specification.

> **for each device** (page 1, line 14 through page 2, line 2 of the specification).

The specification further states:

> Devices with combined programmable logic and high-speed serial channels are increasingly appearing in the marketplace. However, **defining unique pinouts for parts** with different programmable density or different high-speed serial transmission bandwidth **within a family of parts** makes applicability difficult for users (i.e., migration between higher and lower density parts). For example, when a user desires to switch to a transceiver with a larger number of high-speed serial channels, **the board layout for the transceiver chip needs to be changed. Such a change can include the footprint of the transceiver device, routing of the transceiver chip, and/or other affected routing on the board**. Additionally, complex routing and timing issues between the devices will have to be resolved (page 2, lines 3-15 of the specification).

Thus, in light of the specification, one skilled in the art would recognize that devices within a family of devices can have **unique** footprints and layouts (e.g., footprints and layouts can vary or have variations within a family).

One skilled in the art would also be able, in light of the specification, to ascertain the meaning of "where the superset pinout eliminates layout variations within a family of devices." In particular, the specification provides the following example:

> The process 50 (or 50') may allow migration from one member to another member **to not involve changes in footprint or layout** (page 5, lines 17-19 of the specification).

Since migration from one member to another member does not involve layout changes, one skilled in the art would understand that the superset pinout generated by the process 50 (or 50') eliminates layout variations within the family of devices to which the two members belong.

Further examples provided by the specification include:

The method 50 (or 50') **may provide common footprints and layouts for a family of devices** (page 6, lines 12-13 of the specification, emphasis added).

Therefore, the process 50 may provide **a footprint that may be common to all members in the family** and a superset pinout that accommodates the needs of all members (page 8, lines 13-16 of the specification, emphasis added).

In one example, the circuit 100' [FIG. 3] may be another PSI family member with 100K programmable logic gate density and two sets of transceiver channels at 2.5Gbps. The circuit 100' may be InfiniBand compliant (e.g., a serial transceiver function). **In another example, the circuit 100' may have the same footprint and layout, for another member with different locations of no-connect pins** and the transceiver being SONET compliant (page 9, line 19 through page 10, line 6 of the specification, emphasis added).

The process 50 (or 50') may eliminate footprint changes and **reduce or eliminate layout changes when users replace a device with another having different functions for the high-speed serial channels.** The process 50 (or 50') may **reduce or eliminate routing changes when users replace a device with another having a different programmable logic gate density while in the same family, since a common footprint exists for the two members.** Therefore, users **may design board layouts to accommodate for more than one member of a family without external components to allow for later changes, without affecting layout.** The process 50 (or 50') may **reduce or eliminate layout changes when users replace a device with another having a different number of high-speed serial channels while in the same family** (page 11, lines 3-15 of the specification, emphasis added).

The process 50 (or 50') may provide additional cost savings for manufacturers. For example, one device member having one serial channel may call for a single transceiver block. At the same time, another member in the same family may have the same footprint and two transceivers channels (e.g., implement two transceivers blocks). The method 50 (or 50') **may allow the devices to have the same layout**, while the device having fewer channels may not incur the additional cost of a second transceiver block (page 11, line 16 through page 12, line 4 of the specification, emphasis added).

For the reasons presented above, one of ordinary skill in the pertinent art reading the presently pending claims in light of the specification would be able to reasonably ascertain the meets and bounds of the presently claimed invention. As such, claim 19 is fully patentable under 35 U.S.C. §112, second paragraph, and the rejection should be reversed.

4. Group 4 (claim 20) is fully patentable under 35 U.S.C. § 112, second paragraph.

The presently pending claim 20 provides an apparatus comprising a device configured to generate a superset pinout for a family of devices, where (A) the device is further configured to (i) define a pinlist for each device within the family of devices, (ii) generate a superset listing of pins from the pinlist, (iii) create the superset pinout for the family of devices from the superset listing of pins, and (iv) mark each pin of the superset pinout associated with each member of the family of devices, and (B) the superset pinout is configured to reduce layout and footprint changes on a board configured to connect to each member of the family of devices.

The Examiner failed to explicitly state whether the rejection of claim 20 under 35 U.S.C. §112, second paragraph, is based on the failure to claim what the Appellants regard as their invention or on indefiniteness.[83] Therefore, both prongs are addressed for completeness. Whether the claims set forth the subject matter regarded by the Appellants as their invention is a subjective test that is satisfied as evidenced by the submission of claim 20 for examination. The Examiner

[83] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604).

failed to present any evidence or convincing line of reasoning to support a conclusion that the invention set forth in claim 20 is not what the Appellants regard as their invention.[84] The invention set forth in the claims **must be presumed, in the absence of evidence to the contrary, to be that which Appellants regard as their invention.**[85] Since the Examiner presented no evidence or convincing line of reasoning to doubt the invention set forth in claim 20 is what the Appellants regard as their invention, the presumption that the claims are directed to that which the Applicants regard as their invention is intact. As such, claim 20 is patentable under the first prong of 35 U.S.C. §112, second paragraph, and the rejection should be reversed.

With regard to the second requirement above, the recitation in claim 20 of "the superset pinout is configured to reduce layout and footprint changes on a board configured to connect to each member of the family of devices" meets the objective test of defining the metes and bounds of the subject matter by reciting what the superset pinout created by the presently claimed device does. The Examiner's conclusory statement that claim 20 is "incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections" where the "omitted structural cooperative relationship" is "the relation between *layout and footprint changes* and the rest of the claim,"[86] does not provide any analysis of why the scope of claim 20 would not be clear to **a person possessing the ordinary level**

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[84] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604).

[85] MPEP §2172(I), citing *In re Moore*, 439 F.2d 1232, 169 USPQ 236 (C.C.P.A. 1971).

[86] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604).

of skill in the pertinent art when read in light of the specification.[87] In rejecting a claim under the second paragraph of 35 U.S.C. §112, it is incumbent on the Examiner to establish that one of ordinary skill in the pertinent art, when reading the claims in light of the supporting specification, would not have been able to ascertain with a reasonable degree of precision and particularity the particular area set out and circumscribed by the claims.[88] The Examiner has not met the Office's burden to establish that one of ordinary skill in the pertinent art, when reading the claims in light of the supporting specification, would not have been able to ascertain with a reasonable degree of precision and particularity the particular area set out and circumscribed by the claims.[89] As such, claim 20 is patentable under 35 U.S.C. § 112, second paragraph and the rejection should be reversed.

The statement by the Examiner that the claims are "incomplete for omitting essential structural cooperative relationships of elements, such omission amounting to a gap between the necessary structural connections"[90] clearly does not adequately address, *inter alia*, (i) what is considered to be the pertinent art, (ii) what the level of skill is in the pertinent art and (iii) why **one of ordinary skill in the pertinent art, when reading the claims in light of the specification, would not have been able to reasonably ascertain the specific area set out and circumscribed by the claims**. It is not essential to a patentable combination that there be interdependency between

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[87] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003 and paragraph no. 3 of the Detailed Action attached to the Advisory Action dated May 12, 2004 (paper no. 050604). See also MPEP § 2173.02.

[88] *Ex parte Wu*, 10 USPQ2d 2031, 2033 (B.P.A.I. 1989) (citing *In re Moore*, 439 F.2d 1232, 169 USPQ 236 (C.C.P.A. 1971); *In re Hammack*, 427 F.2d 1378, 166 USPQ 204 (C.C.P.A. 1970)).

[89] *Ex parte Wu*, 10 USPQ2d 2031, 2033 (B.P.A.I. 1989) (citing *In re Moore*, 439 F.2d 1232, 169 USPQ 236 (C.C.P.A. 1971); *In re Hammack*, 427 F.2d 1378, 166 USPQ 204 (C.C.P.A. 1970)).

[90] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003.

the elements of the claimed device or that all the elements operate concurrently toward the desired result.[91] Furthermore, a claim does not necessarily fail to comply with 35 U.S.C. §112, second paragraph where the various elements do not function simultaneously, are not directly functionally related, do not directly intercooperate, and/or serve independent purposes.[92] Therefore, the Examiner failed to meet the Office's burden of factually supporting a *prima facie* conclusion that the present claims are not definite. As such, the presently pending claim 20 is fully patentable under the second prong of 35 U.S.C. §112, second paragraph, and the rejection should be reversed.

Furthermore, one of ordinary skill in the art when reading the claims in light of the specification would clearly understand the relationship between the elements of claim 20. Specifically, the meaning of the terms used in the claim is clearly apparent from the prior art or from the specification and drawings as originally filed. In particular, changes would be understood to refer to variations, differences, dissimilarities, etc.[93] With respect to the terms "pinout" and "pinlist," the specification states:

> **Pinout** may refer to a layout of the signals for a device (e.g., a list of physical pins of a device package and functions assigned to those pins). For example, a pinout may be a list of pins and pin functions for quad flat pack (QFP) (e.g., pin1 = ground, pin2 = signal A, etc.) and for a ball grid array (BGA) (e.g., A1=Ground, A2 = signal A, etc.) **Pinlist** may refer to a list of signals for a device to be assigned to physical pins to become the functions of the pins (e.g., the ground, signal A, etc.). For simplicity a BGA ball may also be referred to as a pin (page 6, lines 1-9 of the specification, emphasis added).

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[91] MPEP § 2171.01, citing *Ex parte Nolden*, 149 USPQ 378, 380 (Bd. Pat. App.1965).

[92] MPEP § 2171.01, citing *Ex parte Huber,* 148 USPQ 447, 448-49 (Bd. Pat. App. 1965).

[93] See entry for variation from Merriam-Webster Online Thesaurus attached in the Appendix as Exhibit A.

With respect to the term "footprint," one of ordinary skill in the art would recognize the term "footprint", with respect to a device, to refer to the physical pinout or pattern of pins (or balls) of the device.[94] With respect to the term "layout," one of ordinary skill in the art would recognize the term "layout", with respect to a device, to refer to the physical pinout or pattern of connections to pins (or balls) of the device.[95] One skilled in the art would understand that devices within a family of devices can have different footprints and, therefore, different layouts. For example, the specification states:

> Devices with combined programmable logic and high-speed serial channels are increasingly appearing in the marketplace. However, **defining unique pinouts for parts** with different programmable density or different high-speed serial transmission bandwidth **within a family of parts** makes applicability difficult for users (i.e., migration between higher and lower density parts). For example, when a user desires to switch to a transceiver with a larger number of high-speed serial channels, **the board layout for the transceiver chip needs to be changed. Such a change can include the footprint of the transceiver device, routing of the transceiver chip, and/or other affected routing on the board.** Additionally, complex routing and timing issues between the devices will have to be resolved (page 2, lines 3-15 of the specification, emphasis added).

With respect to the relationship between the elements of claim 20, claim 20 recites the device is further configured to (i) define A PINLIST for each device within the family of devices, (ii) generate A SUPERSET LISTING OF PINS **from** THE PINLIST, and (iii) create THE SUPERSET PINOUT FOR THE FAMILY OF DEVICES **from** THE SUPERSET LISTING OF PINS. Claim 20 further recites that the superset pinout is configured to reduce layout and footprint changes on a board configured to connect to each member of the family of devices. Thus, one of ordinary skill in the

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[94] See Exhibit B in the Appendix for examples of layouts for various footprints.

[95] See Exhibit B in the Appendix for examples of layouts for various footprints.

art would clearly understand the relationship between the elements of claim 20 based on the claim language.

Furthermore, with respect to the relationship between the superset pinout and reducing layout and footprint changes on a board configured to connect to each member of the family of devices, the specification provides an example:

> While in the state 52, the process 50 may **define the pinlist for each device within a family of devices**. The process 50 may define what pins and how many of each are required for each device (**as if generating a unique pinout for that device**). For example, if there are two members in the family for which to create a superset pinout, then the individual pinlist may be:
>
> MEMBERA: AABC (two pins of A)
> MEMBERB: ABD
>
> While in the state 54, the process 50 may generate a superset listing of pins from the individual pinlist (e.g., combining pins that can be shared by more than one member). The process 50 may note which pins are applicable to which device members. Therefore, from the two members MEMBERA and MEMBERB, the superset pinlist may be AABCD (page 6, line 17 through page 7, line 11 of the specification, emphasis added).

The specification further states:

> The present invention may be directed to a method for **generating superset pinout for devices** with combined programmable logic with high-speed serial channels. The method 50 (or 50') **may provide common footprints and layouts for a family of devices** (page 6, lines 10-13 of the specification, emphasis added).

One skilled in the art would clearly understand that creating a superset pinout (e.g., five pins AABCD) that provides a common **footprints and layouts** for each member of a family of devices relates to reducing layout and footprint changes (e.g., four pins AABC for member A and three pins ABD for member B if unique pinouts are implemented) on a board configured to connect to each

member of the family of devices. Thus, one of ordinary skill in the pertinent art reading the presently pending claims in light of the specification would be reasonably apprised of the meets and bounds of the presently claimed invention. Therefore, the Examiner failed to meet the Office's burden of factually supporting a *prima facie* conclusion that the present claims are not definite. As such, the presently pending claim 20 is fully patentable under the second prong of 35 U.S.C. §112, second paragraph, and the rejection should be reversed.

Furthermore, the Examiner's conclusory statement that "layout and footprint changes cannot be reduced where there is first no prior recitation of their existence"[96] does not adequately explain why the scope of the claims would not be clear to **a person possessing the ordinary level of skill in the pertinent art when read in light of the specification**.[97] Specifically, the Examiner fails to clearly state whether the prior recitation she is looking for should appear in (i) the preamble, (ii) the specification or (iii) the other claim elements. The mere fact that the body of a claim recites additional elements which do not appear in the claim's preamble does not render the claim indefinite under 35 U.S.C.112, second paragraph.[98] Furthermore, The mere fact that a term or phrase used in

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[96] See page 3, lines 3-4 of the final Office Action dated December 30, 2003 and page 2, section no. 3, lines 6-7 of the Advisory Action dated March 22, 2004.

[97] See paragraph no. 5 on page 2 of the final Office Action dated December 30, 2003.

[98] MPEP § 2173.05(e), citing *In re Larsen*, No.01-1092 (Fed. Cir. May 9, 2001) (unpublished) (The preamble of the *Larsen* claim recited only a hanger and a loop but the body of the claim positively recited a linear member. The examiner rejected the claim under 35 U.S.C.112, second paragraph, because the omission from the claim 's preamble of a critical element (i.e., a linear member) renders that claim indefinite. The court reversed the examiner 's rejection and stated that the totality of all the limitations of the claim and their interaction with each other must be considered to ascertain the inventor 's contribution to the art. Upon review of the claim in its entirety, the court concluded that the claim at issue apprises one of ordinary skill in the art of its scope and, therefore, serves the notice function required by 35 U.S.C.112, paragraph 2.).

the claims has no antecedent basis in the specification disclosure does not mean, necessarily, that the term or phrase is indefinite.[99] There is no requirement that the words in the claims must match those used in the specification disclosure.[100] The MPEP states:

> The Examiner's task of making sure the claim language complies with the requirements of the statute should be carried out in a positive and constructive way, so that minor problems can be identified and easily corrected, and so that the major effort is expended on more substantive issues.[101]

With respect to carrying out the Examiner's task, the MPEP provides that the Examiner should "suggest corrections to antecedent problems."[102] Furthermore, the MPEP states:

> In reviewing a claim for compliance with 35 U.S.C. 112, second paragraph, the examiner must consider the claim as a whole to determine whether the claim apprises one of ordinary skill in the art of its scope and, therefore, serves the notice function required by 35 U.S.C.112, second paragraph, by providing clear warning to others as to what constitutes infringement of the patent. See, e.g., *Solomon v. Kimberly-Clark Corp.*, 216 F.3d 1372, 1379, 55 USPQ2d 1279, 1283 (Fed. Cir. 2000). If the language used by Applicant satisfies the statutory requirements of 35 U.S.C. 112, second paragraph, but the Examiner merely wants the Applicant to improve the clarity or precision of the language used, the claim must not be rejected under 35 U.S.C.112, second paragraph, rather, **the examiner should suggest improved language to the Applicant**.[103]

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[99] MPEP § 2173.05.

[100] *Id.*

[101] MPEP § 2173.05(e) EXAMINER SHOULD SUGGEST CORRECTION TO ANTECEDENT PROBLEMS.

[102] *Id.*

[103] MPEP §2173.02, emphasis added.

Contrary to the Patent Office's policy as expressed in the MPEP, the Examiner has refused numerous invitation by Appellant's representatives to suggest corrections that would be acceptable.

Furthermore, the Appellant's representative has made an extensive effort to provide claim language to which the Examiner will not object. However, the Examiner appears to want Appellants to keep guessing at what language will ultimately be acceptable. Specifically, Appellant's representative spent two hours in a telephone interview with the Examiner trying to resolve the rejection.[104] Appellant's representative followed up the two hour telephone interview by submitting a proposed amendment containing language which was believed to have been agreed to by the Examiner.[105] The Examiner's response was a cryptic reply that "the response does not place this application in a condition for allowance."[106] When Appellant's representative asked the Examiner to clarify whether the amendment was what had been agreed to, the Examiner again cryptically replied "Partially. There is still more work to be done."[107] An Amendment After Final was filed on March 22, 2004 which included amendments that Appellants believed would overcome the § 112 rejection. The Amendment After Final was entered, however, the Examiner maintained the § 112 rejections.[108] Although Appellant's representatives made further attempts to determine what the Examiner was seeking, the Examiner refused to discuss any further what language she

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[104] See Interview Summary dated March 8, 2004 (paper no. 6).

[105] See e-mail message dated February 26, 2004, attached as Exhibit C in the Appendix.

[106] See e-mail message dated February 27, 2004, attached as Exhibit D in the Appendix.

[107] See e-mail message dated February 27, 2004, attached as Exhibit E in the Appendix.

[108] See Advisory Action dated May 12, 2004 (paper no. 050604).

would find acceptable. The Examiner's responses clearly were not suggestions for corrections or improved language as encouraged by the MPEP.

In yet another effort to materially advance the prosecution of the application, Appellant's representatives took the extraordinary step of asking the Examiner's supervisor whether he could suggest a correction or improved language in light of the Examiner's statements. The Examiner's supervisor stated:

> . . . an earlier reference in the claims was needed to provide "structural connection" for layout variations or footprint variation.[109]

Although Appellant's representative did not necessarily agree with the solution proposed by the Examiner's supervisor, in a last attempt to materially advance the prosecution of the application to allowance, a second Amendment After Final was filed on May 27, 2004 in which an earlier reference in the claim 20 was made for layout and foot variations. Specifically, the currently pending claim 20 reads as follows:

> 20. An apparatus comprising:
> a device configured to generate a superset pinout for a family of devices, wherein (A) said device is further configured to (i) define a pinlist for each device within said family of devices, (ii) generate a superset listing of pins from said pinlist, (iii) create said superset pinout for said family of devices from said superset listing of pins, and (iv) mark each pin of said superset pinout associated with each member of said family of devices, and (B) said superset pinout is configured to reduce layout and footprint changes on a board configured to connect to each member of said family of devices.

The amended claim 20 submitted in the Amendment After Final filed May 27, 2004 read as follows:

> 20. (CURRENTLY AMENDED) An apparatus comprising:
> a device configured to generate a superset pinout for a family of devices <u>having layout and footprint variations</u>, wherein (A) said

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[109] *Id.*

> device is further configured to (i) define a pinlist for each device within said family of devices, (ii) generate a superset listing of pins from said pinlist, (iii) create said superset pinout for said family of devices from said superset listing of pins, and (iv) mark each pin of said superset pinout associated with each member of said family of devices, and (B) said superset pinout is configured to reduce layout and footprint changes on a board configured to connect to each member of said family of devices.

In an Advisory Action, the Examiner stated that the Amendment After Final[110] would not be entered because:

> the added limitation, "having footprint variations" in the independent claims, narrows the scope of the claims. Therefore, further consideration and/or search is required..[111]

However, the file history is clear that considerable consideration has already been given. In particular, the Examiner presumably performed a thorough search[112] and had previously indicated that "reducing or eliminating layout and footprint changes on a board between a family of devices" was allowable subject matter.[113] Specifically, claim 5 as originally filed recited:

> 5. The method according to claim 1, wherein step (C) further comprises:
> eliminating **footprint variations** within said family of devices with said superset pinout.

Claim 6 as originally presented recited:

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[110] Filed May 27, 2004.

[111] See page 2 of the Advisory Action dated July 12, 2004 (paper no. 070804).

[112] See 37 CFR1.104(a)(1); (On taking up an application for examination . . the examiner shall make a thorough study thereof and shall make a thorough investigation of the available prior art relating to the subject matter of the claimed invention . . . .).

[113] See page 5, Allowable Subject Matter, in the Office Action dated July 14, 2003 (paper no. 3).

> 6. The method according to claim 1, wherein step (C) further comprises:
>
> eliminating **layout variations** within said family of devices with said superset pinout.

The Examiner stated that the originally presented claims 5 and 6 contained allowable subject matter.[114] The Examiner has already considered and/or searched footprint and layout variations and found them allowable over the art of record. It is Appellant's understanding that the Examiner would not indicate particular claims are allowable without sufficient consideration and/or search. Furthermore, the Examiner's remark does not fully address the specific added phrase "having layout and footprint variations." Furthermore, the Examiner failed to address whether the added phrase provided the earlier reference which the Examiner had asserted was needed.

Contrary to the position taken by the Examiner, one skilled in the art would be able to ascertain the meaning of the phrase "the superset pinout is configured to reduce layout and footprint changes on a board configured to connect to each member of the family of devices" in light of the specification. The test for definiteness under 35 U.S.C.112, second paragraph, is whether "those skilled in the art would understand what is claimed when the claim is read in light of the specification."[115] If one skilled in the art is able to ascertain the meaning of the phrase "the superset pinout is configured to reduce layout and footprint changes on a board configured to connect to each member of the family of devices" in light of the specification, 35 U.S.C.112, second paragraph, is

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[114] See page 5, Allowable Subject Matter, in the Office Action dated July 14, 2003 (paper no. 3).

[115] *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 USPQ2d 1081, 1088 (Fed. Cir. 1986).

satisfied.[116] Despite the position taken by the Examiner, one skilled in the art would be able to ascertain the meaning of the phrase "the superset pinout is configured to reduce layout and footprint changes on a board configured to connect to each member of the family of devices" in light of the specification. As such, claim 20 is fully patentable under 35 U.S.C. § 112, second paragraph, and the rejection should be reversed.

Specifically, one **skilled** in the art would understand that the existence of layout and footprint changes is implied by the statement that the superset pinout is configured to reduce layout and footprint changes. Therefore, a separate recitation of their existence or creation is not necessary. Furthermore, one skilled in the art would further recognize that layout and footprint changes may be reduced by preventing their creation to begin with. Thus, requiring that the claims include a recitation of the creation of layout and footprint changes would not result in a clear and distinct claiming of the invention. Furthermore, one skilled in the art would be able to ascertain the meaning of the phrase "the superset pinout is configured to reduce layout and footprint changes on a board configured to connect to each member of the family of devices" in light of the specification. The specification includes two drawings (e.g., FIGS. 2 and 3) which show example layouts (or footprints) for different members of a family of devices.[117] Furthermore, the specification states:

> **Transceiver devices (or the like) with varying number of channels have unique pinouts to accommodate the varying I/O requirements.** However, increasing the number of pins increases power consumption. Larger numbers of channels also need additional die space. Furthermore, **programmable logic devices (PLDs) and transceiver devices are typically mounted in separate**

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[116] MPEP § 2173.02.

[117] See the description of FIGS. 2 and 3 on page 9, line 4 through page 10, line 6 of the specification.

> **packages to accommodate unique I/O packaging requirements for each device** (page 1, line 14 through page 2, line 2 of the specification, emphasis added).

The specification further states:

> Devices with combined programmable logic and high-speed serial channels are increasingly appearing in the marketplace. However, **defining unique pinouts for parts** with different programmable density or different high-speed serial transmission bandwidth **within a family of parts** makes applicability difficult for users (i.e., migration between higher and lower density parts). For example, when a user desires to switch to a transceiver with a larger number of high-speed serial channels, **the board layout for the transceiver chip needs to be changed. Such a change can include the footprint of the transceiver device, routing of the transceiver chip, and/or other affected routing on the board**. Additionally, complex routing and timing issues between the devices will have to be resolved (page 2, lines 3-15 of the specification, emphasis added).

Thus, in light of the specification, one skilled in the art would recognize that devices within a family of devices can have unique footprints and layouts and that when a family of devices has different footprints and/or layouts, footprint and layout changes may be needed when switching between two devices. One skilled in the art would also be able, in light of the specification, to ascertain the meaning of "the superset pinout is configured to reduce layout and footprint changes on a board configured to connect to each member of a family of devices." In particular, the specification provides the following example:

> The process 50 (or 50') [which generates a superset pinout] may allow migration from one member to another member **to not involve changes in footprint or layout** (page 5, lines 17-19 of the specification, emphasis added).

Since migration from one member to another member does not involve layout changes, one skilled in the art would understand that the superset pinout generated by the process 50 (or 50') reduces

layout and footprint changes to a board configured to connect to each member of the family of devices to which the two members belong.

> Further examples provided by the specification include:
>
> The method 50 (or 50') **may provide common footprints and layouts for a family of devices** (page 6, lines 12-13 of the specification, emphasis added).
>
> Therefore, the process 50 may provide a footprint that may be common to all members in the family and **a superset pinout that accommodates the needs of all members** (page 8, lines 13-16 of the specification, emphasis added).
>
> In one example, the circuit 100' [FIG. 3] may be another PSI family member with 100K programmable logic gate density and two sets of transceiver channels at 2.5Gbps. The circuit 100' may be InfiniBand compliant (e.g., a serial transceiver function). **In another example, the circuit 100' may have the same footprint and layout, for another member with different locations of no-connect pins** and the transceiver being SONET compliant (page 9, line 19 through page 10, line 6 of the specification, emphasis added).
>
> The process 50 (or 50') may eliminate footprint changes and **reduce or eliminate layout changes when users replace a device with another having different functions for the high-speed serial channels.** The process 50 (or 50') may **reduce or eliminate routing changes when users replace a device with another having a different programmable logic gate density while in the same family, since a common footprint exists for the two members.** Therefore, users **may design board layouts to accommodate for more than one member of a family without external components to allow for later changes, without affecting layout.** The process 50 (or 50') may **reduce or eliminate layout changes when users replace a device with another having a different number of high-speed serial channels while in the same family** (page 11, lines 3-15 of the specification, emphasis added).
>
> The process 50 (or 50') may provide additional cost savings for manufacturers. For example, one device member having one serial channel may call for a single transceiver block. At the same time, another **member in the same family may have the same footprint** and two transceivers channels (e.g., implement two transceivers

> blocks). The method 50 (or 50') **may allow the devices to have the same layout**, while the device having fewer channels may not incur the additional cost of a second transceiver block (page 11, line 16 through page 12, line 4 of the specification, emphasis added).

For the reasons presented above, one of ordinary skill in the pertinent art reading the presently pending claims in light of the specification would be able to reasonably ascertain the meets and bounds of the presently claimed invention. As such, claim 20 is fully patentable under 35 U.S.C. §112, second paragraph, and the rejection should be reversed.

B. <u>The groupings of the claims are proper under 37 C.F.R. § 1.192(c)(7) where each group can be found patentable upon a different ground from each other group</u>

During prosecution, each independent and dependent claim is considered to be separately patentable over every other claim.[118] For the reasons presented below, each of the groups is considered to be separately patentable over every other group and, therefore, the groupings of the claims is proper under 37 C.F.R §1.192(c)(7).[119]

Specifically, the claims in group 1 and group 2 are directed to a method while the claims of groups 3 and 4 are directed to apparatus. Furthermore, the Examiner cited different reasons for the rejections with respect to each of the groups 1-4. Therefore, the arguments against the rejection under 35 U.S.C. § 112, second paragraph, with respect to each of the groups necessarily

---

[118] See, e.g., *Rowe v. Dror*, 42 USPQ2d 1550, 1552 (Fed. Cir. 1997), *Preemption Devices, Inc. v. Minnesota Mining and Manufacturing Company*, 221 USPQ 841, 843 (Fed. Cir. 1984), and *Jones v. Hardy*, 727 F.2d 1524, 1528, 220 USPQ 1021, 1024 (Fed. Cir. 1984) (It is well established that each claim in a patent constitutes a separate invention.).

[119] Manual of Patent Examining Procedure (M.P.E.P.), Eighth Edition, Revision 2, May 2004, §1206.

involve determination based upon different facts. Since the arguments with respect to each of the groups involve different facts, the separate groupings of claims are believed to be proper.

C. CONCLUSION

For the reasons presented above, because those skilled in the art would understand what is claimed when the presently pending claims are read in light of the specification,[120] the presently pending claims 1-4, 6-11 and 13-20 are patentable under the second paragraph of 35 U.S.C. §112. Hence, the Examiner has clearly erred with respect to the patentability of the claimed invention. It is respectfully requested that the Board overturn the Examiner's rejection of all pending claims, and hold that the claims are patentable under 35 U.S.C. §112.

Respectfully submitted,

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Christopher P. Maiorana
Reg. No. 42, 829

Dated: September 1, 2004

24840 Harper Avenue
Suite 100
St. Clair Shores, MI 48080
(586) 498-0670

[120] *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576, 1 USPQ2d 1081, 1088 (Fed. Cir. 1986).

IX. APPENDIX

The claims of the present application which are involved in this appeal are as follows:

1. A method for generating a superset pinout for a family of devices, comprising the steps of:

(A) defining a pinlist for each device within said family of devices;

(B) generating a superset listing of pins from said pinlist;

(C) creating said superset pinout for said family of devices from said superset listing of pins to eliminate potential footprint variations within said family of devices; and

(D) marking each pin of said superset pinout associated with each member of said family of devices.

2. The method according to claim 1, wherein step (D) further comprises;

customizing a superset grid according to said superset listing of pins.

3. The method according to claim 2, wherein step (D) further comprises:

marking a specific pin in said superset grid for each member of said family of devices in response to the customizing.

4. The method according to claim 1, wherein said family of devices comprises devices with combined programmable logic and high-speed serial channels.

5. (CANCELED).

6. The method according to claim 1, wherein step (C) further comprises:

eliminating potential layout variations within said family of devices with said superset pinout.

7. The method according to claim 1, wherein step (B) further comprises:

combining pins shared by more than one member of said family of devices.

8. The method according to claim 1, wherein step (C) further comprises:

allocating a pin for each signal in said pinlist.

9. The method according to claim 1, wherein step (C) further comprises:

providing a common footprint to each member of said family of devices.

10. The method according to claim 1, wherein step (C) further comprises:

designing a board layout (i) to accommodate more than one member of said family of devices and (ii) to allow for late changes without affecting said board layout and without external components.

11. The method according to claim 1, wherein step (C) further comprises:

limiting each pin of said superset pinout to a single function.

12. (CANCELED).

13. The method according to claim 1, wherein step (D) further comprises:
marking one or more pins no-connect for a particular member device.

14. The method according to claim 1, wherein said family of devices comprise programmable logic and high-speed serial channel devices.

15. The method according to claim 1, wherein step (C) further comprises:
allowing for migration of devices within said family of devices.

16. The method according to claim 1, wherein step (C) further comprises:
allowing for migration to higher gate densities.

17. The method according to claim 1, wherein step (C) further comprises:
allowing for migration to increased bandwidth channels.

18. The method according to claim 1, wherein step (C) further comprises:
reducing layout and footprint changes on a board configured to connect to said members of said family of devices.

19. An apparatus for generating a superset pinout for a family of devices comprising:

means for defining a pinlist for each device within said family of devices;

means for generating a superset listing of pins from said pinlist;

means for creating said superset pinout for said family of devices from said superset listing of pins, wherein said superset pinout eliminates layout variations within said family of devices; and

means for marking each pin of said superset pinout associated with each member of said family of devices.

20. An apparatus comprising:

a device configured to generate a superset pinout for a family of devices, wherein (A) said device is further configured to (i) define a pinlist for each device within said family of devices, (ii) generate a superset listing of pins from said pinlist, (iii) create said superset pinout for said family of devices from said superset listing of pins, and (iv) mark each pin of said superset pinout associated with each member of said family of devices, and (B) said superset pinout is configured to reduce layout and footprint changes on a board configured to connect to each member of said family of devices.

Merriam-Webster Online Thesaurus

Dictionary

One entry found for **variation**.

Entry Word: **variation**
Function: *noun*
Text: **1**
Synonyms CHANGE 1, alteration, modification, mutation, turn
Related Word difference, dissimilarity; deflection, discrepancy
Contrasted Words stability, unchangeableness
2
Synonyms VARIANCE 1, difference
Related Word shift; divergence; discrepancy, disparity
Contrasted Words uniformity

For **More Information on "variation" go to Britannica.com**
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Thesaurus Symbols

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WORD GAMES
WORD FOR THE WISE
ONLINE STORE
HELP
Merriam-Webster Inc. Company information

Merriam-Webster Online Dictionary

Thesaurus

3 entries found for **variation**.
To select an entry, click on it.

variation
direct variation
inverse variation
Go

Main Entry: **var·i·a·tion**
Pronunciation: "ver-E-'A-sh&n, "var-
Function: *noun*
1 a : the act or process of varying **:** the state or fact of being varied **b :** an instance of varying **c :** the extent to which or the range in which a thing varies
2 : DECLINATION 6
3 a : a change of algebraic sign between successive terms of a sequence **b :** a measure of the change in data, a variable , or a function
4 : the repetition of a musical theme with modifications in rhythm, tune, harmony, or key
5 a : divergence in the characteristics of an organism from the species or population norm or average **b :** something (as an individual or group) that exhibits variation
6 a : a solo dance in classic ballet **b :** a repetition in modern ballet of a movement sequence with changes
- **var·i·a·tion·al** /-shn&l, -sh&-n&l/ *adjective*
- **var·i·a·tion·al·ly** *adverb*

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Pronunciation Symbols

Merriam-Webster Online Dictionary

One entry found for **vary**.

Main Entry: **vary**
Pronunciation: 'ver-E, 'var-
Function: *verb*
Inflected Form(s): **var·ied**; **vary·ing**
Etymology: Middle English *varien,* from Middle French or Latin; Middle French *varier,* from Latin *variare,* from *varius* various
transitive senses
1 a : to make a partial change in **:** make different in some attribute or characteristic **b :** to make differences between items in **:** DIVERSIFY
2 : to present under new aspects <*vary* the rhythm and harmonic treatment>
intransitive senses
1 : to exhibit or undergo change <the sky was constantly *varying*>
2 : DEVIATE, DEPART
3 : to take on successive values <*y varies* inversely with *x*>
4 : to exhibit divergence in structural or physiological characters from the typical form
synonym see CHANGE
- vary·ing·ly /-i[ng]-lE/ *adverb*

Merriam-Webster Online Dictionary

Thesaurus

One entry found for **diverse**.

Main Entry: **di·verse**
Pronunciation: `dI-'v&rs, d&-', 'dI-"`
Function: *adjective*
Etymology: Middle English *divers, diverse,* from Old French & Latin; Old French *divers,* from Latin *diversus,* from past participle of *divertere*
1 : differing from one another **:** UNLIKE
2 : composed of distinct or unlike elements or qualities
synonym see DIFFERENT
- di·verse·ly *adverb*
- di·verse·ness *noun*

For **More Information on "diverse" go to Britannica.com**

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Pronunciation Symbols

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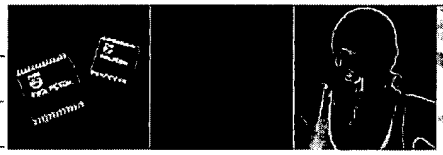
0.8mm pitch BGA adapter matches device footprint

BGA socketing adapter has 0.8mm pitch and is available in wide range of footprints to match device to be attached. Solder balls reflow at standard SMT process temperatures and coplanarity is consistently under 0.152mm.
ADVANCED INTERCONNECTIONS
http://www.advintcorp.com/

MultiMarket Semiconductors

MultiMarket Semiconductors
Standard analog
• Product catalog and datasheets
• Featured products
• Documentation
• Packaging
Package Overview
• Sales Offices & Distributors
• Product Selector



Chip scale packaging: the ultimate in package miniaturization

Key benefits | Key features | Key applications | Information resources | Product overview

Helping to optimize board space design, Philips offers a number of analog products - including system resets, low dropout (LDO) voltage regulators and temperature sensors - in an innovative chip scale package (CSP). These new products use a process where all the devices on a wafer are packaged before dicing, enabling products to be the same size as the dies themselves. This shrinks device footprints to a minimum - maximizing the functionality you can squeeze into your system.

Requiring no interposer or underfill, the *Ultra* CSP is an extremely cost-effect packaging option. It is also very easy to handle, being compatible with standard surface mount techniques and insensitive to moisture, so no special precautions are required before reflowing. Furthermore, as electrical contact with the board is made via solder balls on its base rather than leads, lead coplanarity issues are completely eliminated.

Key benefits

- Significantly reduced device footprint for optimal use of board space
- Cost savings
- Eliminates handling and lead coplanarity problems
- Reduced thermal resistance
- Lower construction material requirements

Key features

- Component is the same size as die
- Short thermal path from die to board
- Board contact by alloy balls directly on the surface
- Moisture insensitive

Key applications

- Battery-powered devices
- Microprocessor applications
- Personal / portable electronics
- Cordless / mobile phones
- Industrial tools

Information resources

PDF Low dropout regulators in chip scale packaging

Product overview

A selection from our range of CSP-housed analog products.

INFO LP2985A-xxUK - 150 mA LDO voltage regulator
INFO MAX8877-xxUK / MAX8878-xxUK - 150 mA LDO voltage regulator
INFO SA57000-xxUK - CapFREE™ voltage regulator
INFO SA57017-xxUK - CapFREE™ voltage regulator

MAX640x - ultra-low power system resets

Ultra CSP® is a trademark of Kulicke & Soffa Investments, Inc.

Attachment A
Parts List and Footprint information for Wafer Scale CSP Reliability Test Board

Alcatel

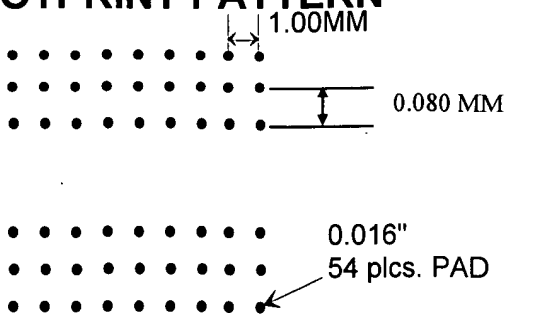
Parts List for Wafer Scale CSP Test Board (HDPUG)

Alcatel Test Part Number	Supplier	#I/O	Pitch (mm)	Part Name (if any)	Comments	
WS-0.8X1-54P	Amkor	54	0.8 x 1.0	WSCSP		
BGA-1.27-256P	Amkor	256	1.27		Control (from CSP TB)	
WCSP-0.75-48P	Fujitsu	48	0.75	SuperCSP48		
SBGA-0.8-40P	Shellcase (NSC)	40	0.8	ShellOp		
SBGA-0.75-46P	Shellcase	46	0.75	Flash		
WS-0.5-6P	Shellcase	6	0.5	ShellBGA CSP		
WS-1.0x1.2-8P	Shellcase	8	1.0x1.2	ShellBGA (EEPROM)		
WS-0.5-4P	NSC	4	0.5	MicroSMD		
WS-0.5-8P	NSC	8	0.5	MicroSMD		
WS-0.5-10P	NSC	10	0.5	MicroSMD		
WS-0.5-12P	NSC	12	0.5	MicroSMD		
WS-0.5-12-98P	FCT	98	0.5	UltraCSP 50	12mil pad	
WS-0.5-10-98P	FCT	98	0.5	UltraCSP 50	10 mil pad	
WS-0.75-46P	FCT	46	0.75	UltraCSP 75		
DP-1x0.4-8P	KOA-Speer	8	1.0x0.4	Die Pack		
DP-1x0.4-24P	KOA-Speer	24	1.0x0.4	Die Pack		
DP-1x0.5-8P	KOA-Speer	8	1.0x0.5	Die Pack		
DP-1x0.5-24P	KOA-Speer	24	1.0x0.5	Die Pack		
DP-1x0.6-8P	KOA-Speer	8	1.0x0.6	Die Pack		
DP-1x0.6-24P	KOA-Speer	24	1.0x0.6	Die Pack		

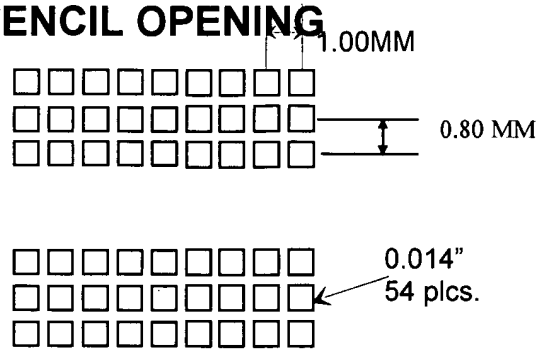
FOOTPRINT AND STENCIL OPENING
FOR 54 PIN CSP 1.00MM AND 0.80 MM (Amkor)

WS-0.8X1-54P

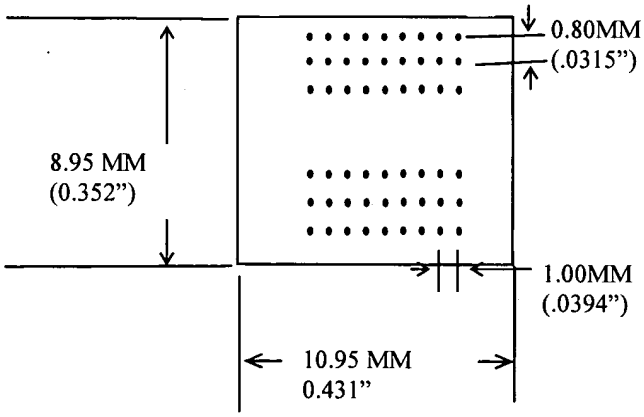
FOOTPRINT PATTERN



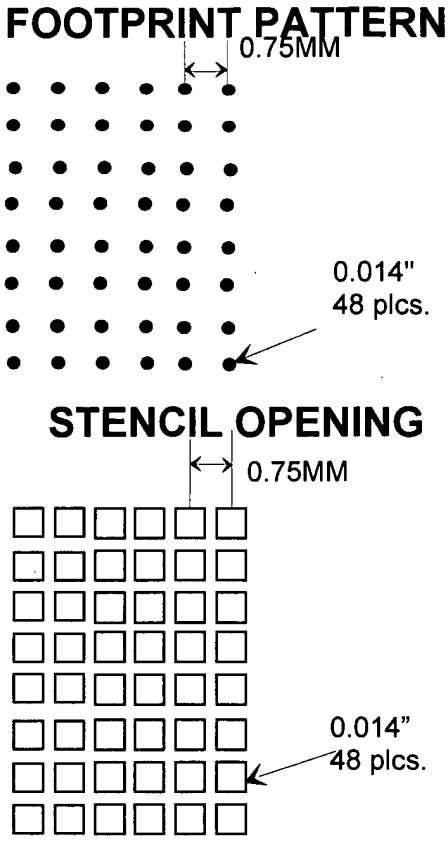
STENCIL OPENING



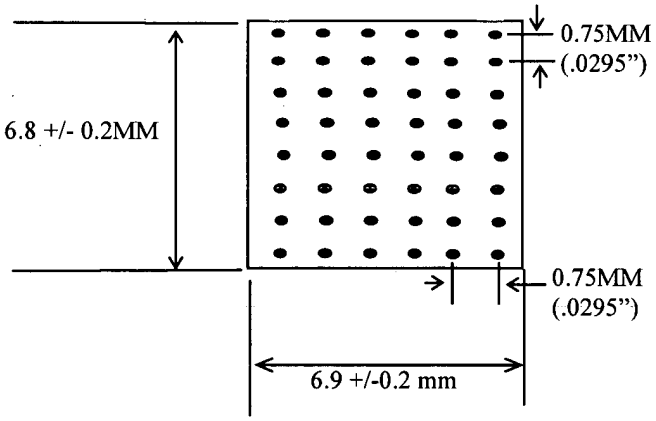
SUPPLIER PART SPECIFICATIONS CSP



FOOTPRINT AND STENCIL OPENING
FOR 48 PIN BGA .75MM (Fujitsu Super CSP48)



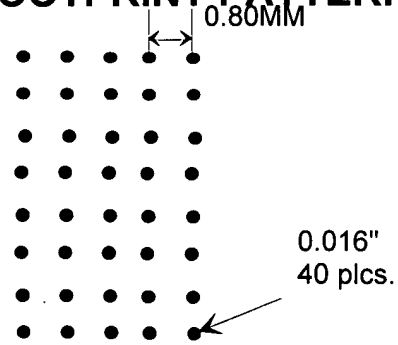
SUPPLIER PART SPECIFICATIONS BGA



FOOTPRINT AND STENCIL OPENING
FOR 40 PIN Shell BGA .80MM

SBGA-0.8-40P

FOOTPRINT PATTERN



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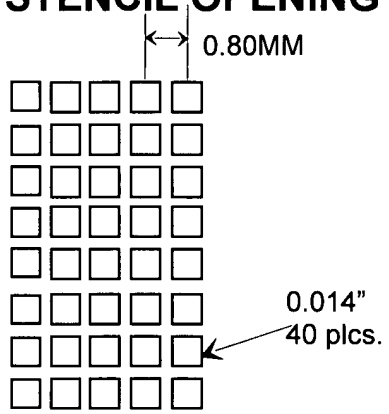
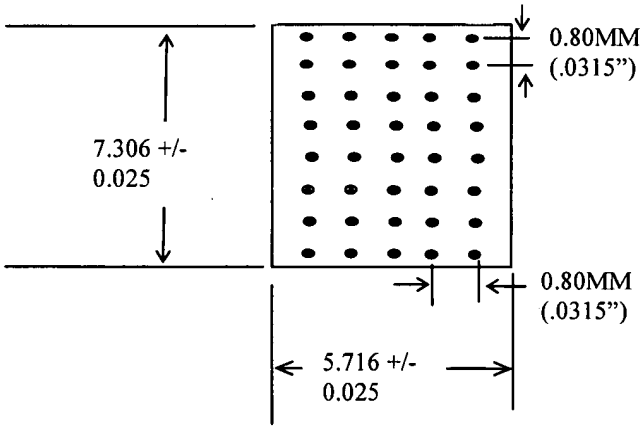
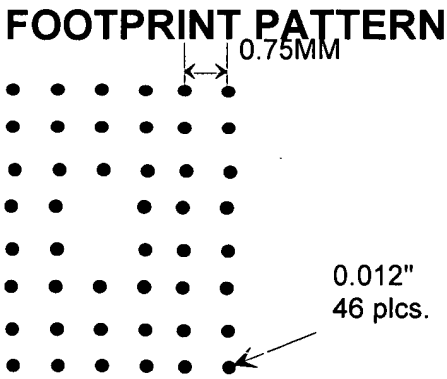
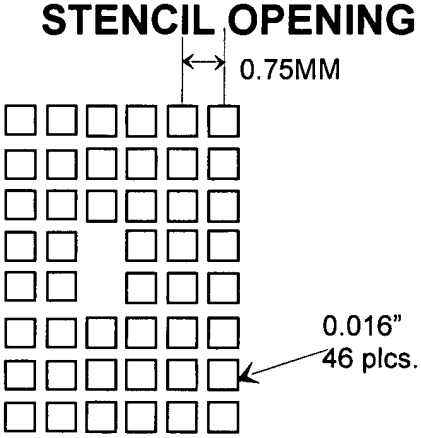


SUPPLIER PART SPECIFICATIONS BGA

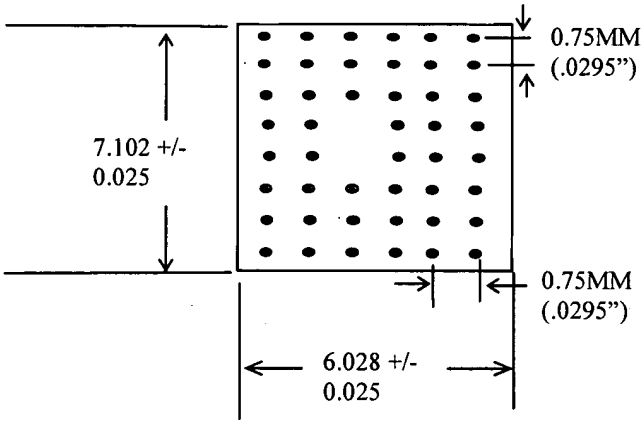


FOOTPRINT AND STENCIL OPENING FOR 46 PIN FLASH .75MM (Shellcase)



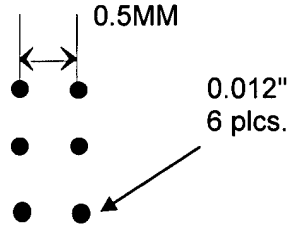


SUPPLIER PART SPECIFICATIONS BGA



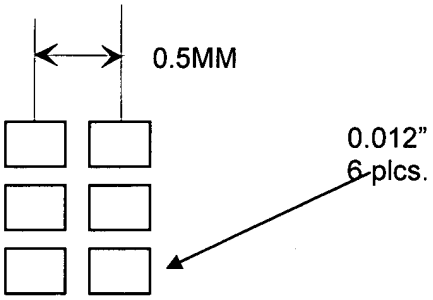
FOOTPRINT AND STENCIL OPENING
FOR 6 PIN CSP .5MM (Shellcase)

FOOTPRINT PATTERN

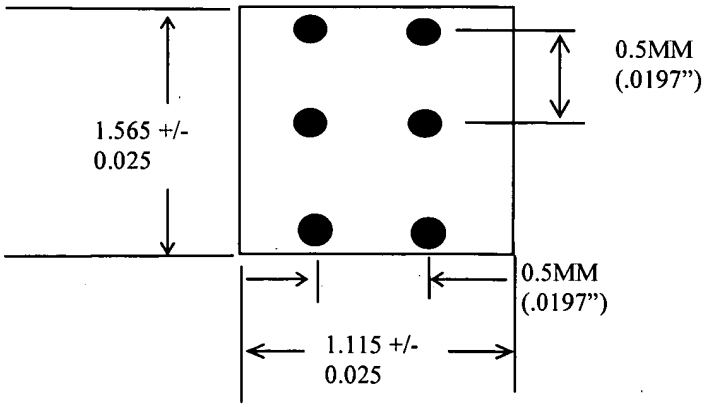


WS-0.5-6P

STENCIL OPENING

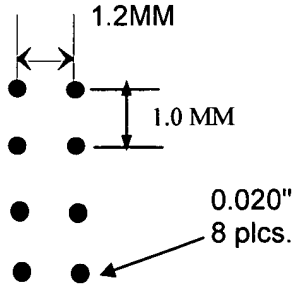


SUPPLIER PART SPECIFICATIONS CSP



FOOTPRINT AND STENCIL OPENING
FOR 8 PIN EEPROM CSP 1.0x1.2MM (Shellcase)

FOOTPRINT PATTERN



WS-1.0x1.2-8P

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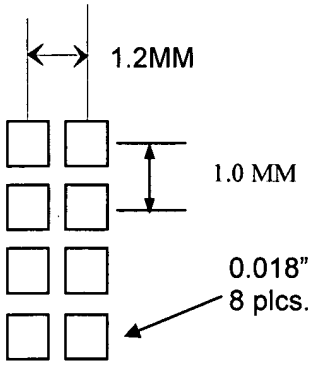
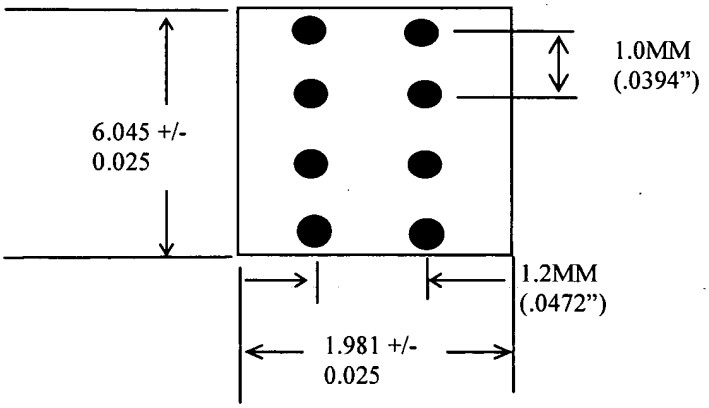


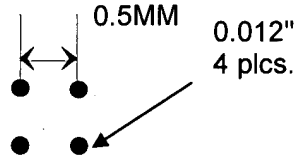
SUPPLIER PART SPECIFICATIONS CSP



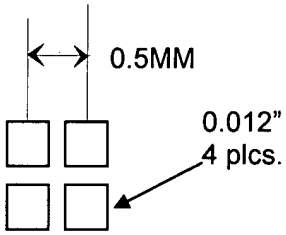
FOOTPRINT AND STENCIL OPENING
FOR 4 BUMP MICRO SMD .5MM (NSC)

WS-0.5-4P

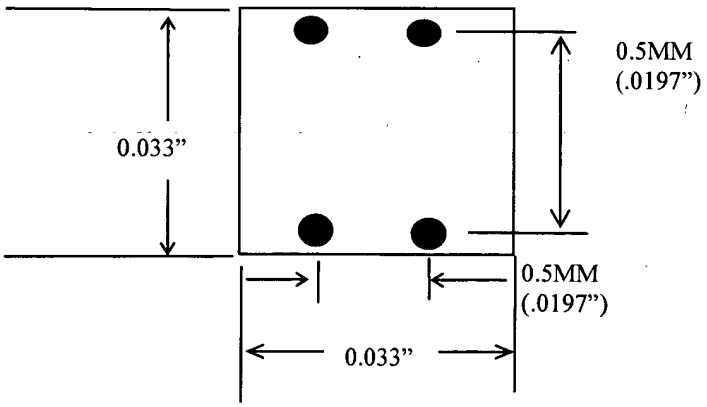
FOOTPRINT PATTERN



STENCIL OPENING



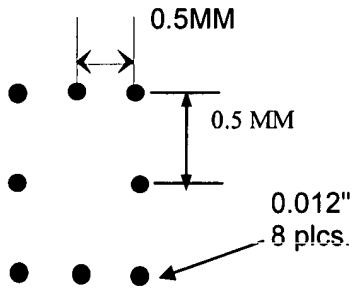
SUPPLIER PART SPECIFICATIONS CSP



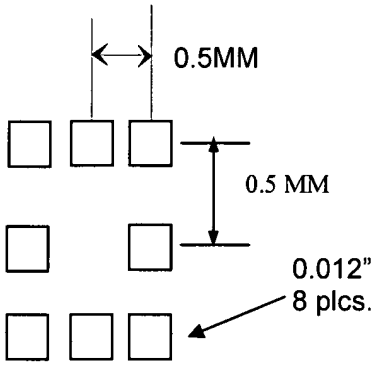
FOOTPRINT AND STENCIL OPENING FOR 8 BUMP MICRO SMD .5MM (NSC)

FOOTPRINT PATTERN

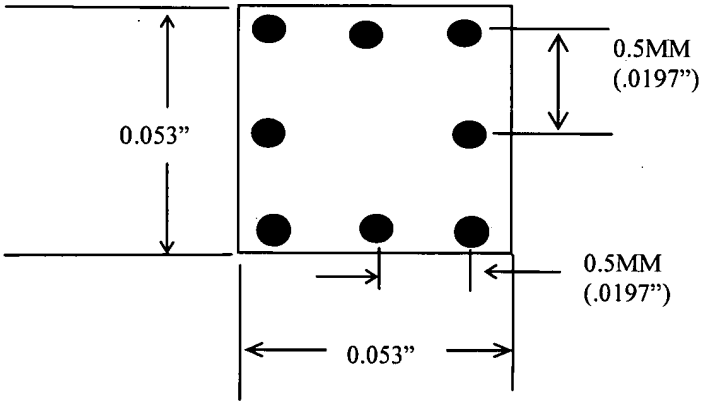
WS-0.5-8P



STENCIL OPENING

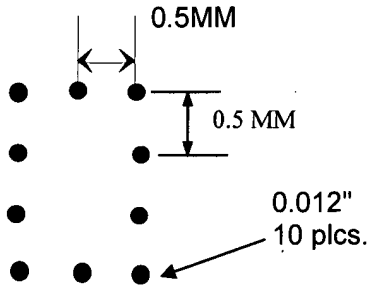


SUPPLIER PART SPECIFICATIONS CSP

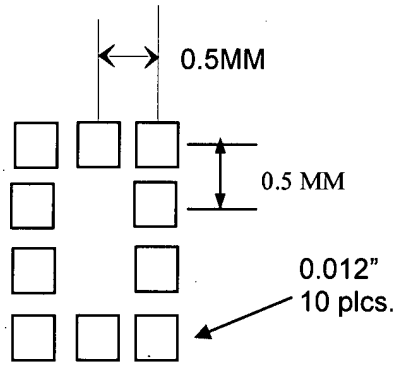


FOOTPRINT AND STENCIL OPENING FOR 10 BUMP MICRO SMD .5MM (NSC)

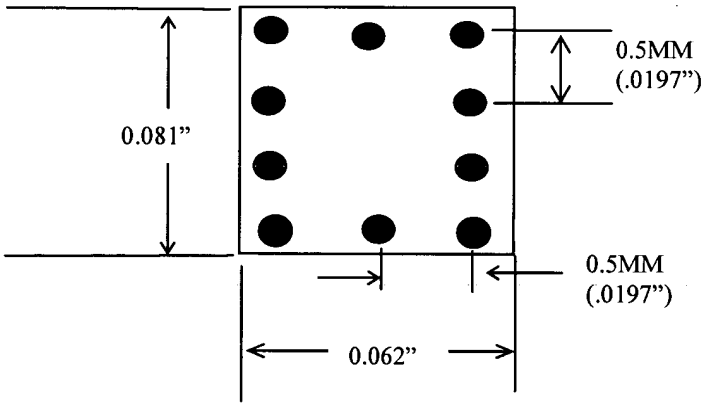
FOOTPRINT PATTERN *WS-0.5-10P*



STENCIL OPENING

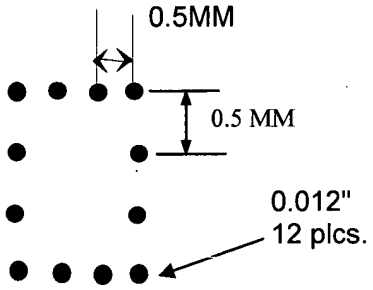


SUPPLIER PART SPECIFICATIONS CSP

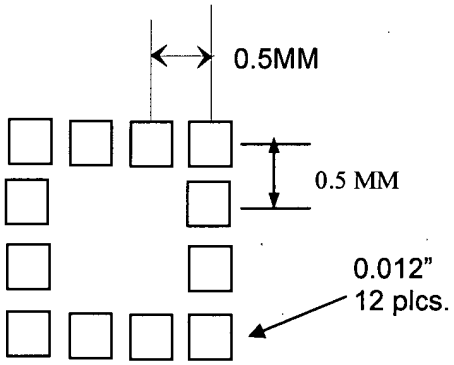


FOOTPRINT AND STENCIL OPENING FOR 12 BUMP MICRO SMD .5MM (NSC)

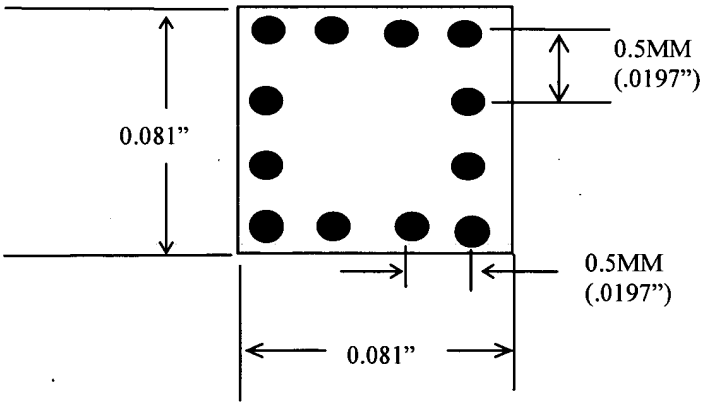
FOOTPRINT PATTERN *WS-0.5-12P*



STENCIL OPENING



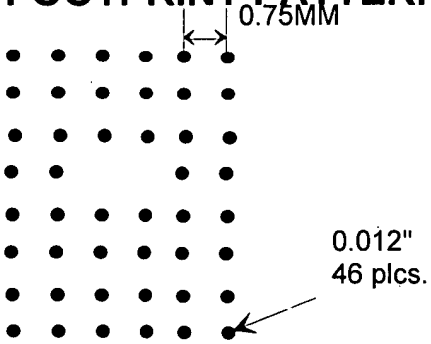
SUPPLIER PART SPECIFICATIONS CSP



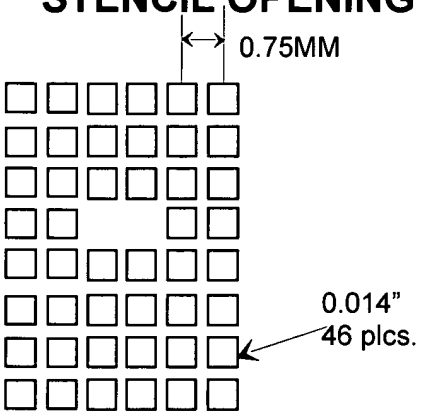
FOOTPRINT AND STENCIL OPENING
FOR 46 PIN BGA .75MM (FCT UltraCSP75)

FOOTPRINT PATTERN

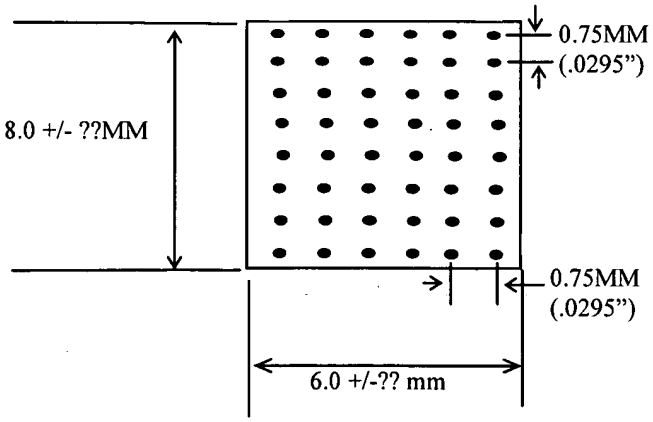
WS-0.75-46P



STENCIL OPENING

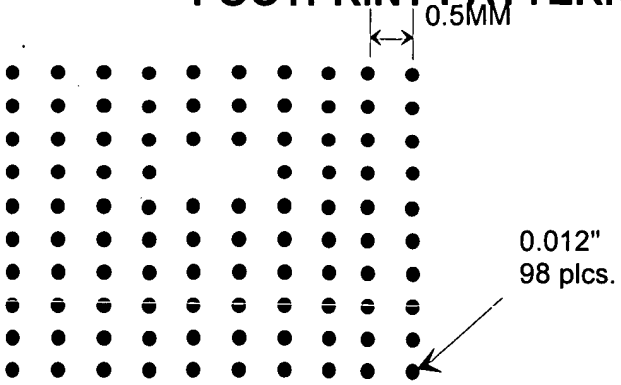


SUPPLIER PART SPECIFICATIONS BGA

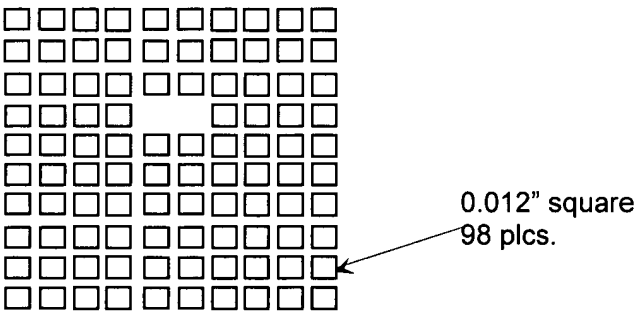


FOOTPRINT AND STENCIL OPENING
FOR 98 PIN BGA .5MM (FCT UltraCSP50 - 12 mil pad)

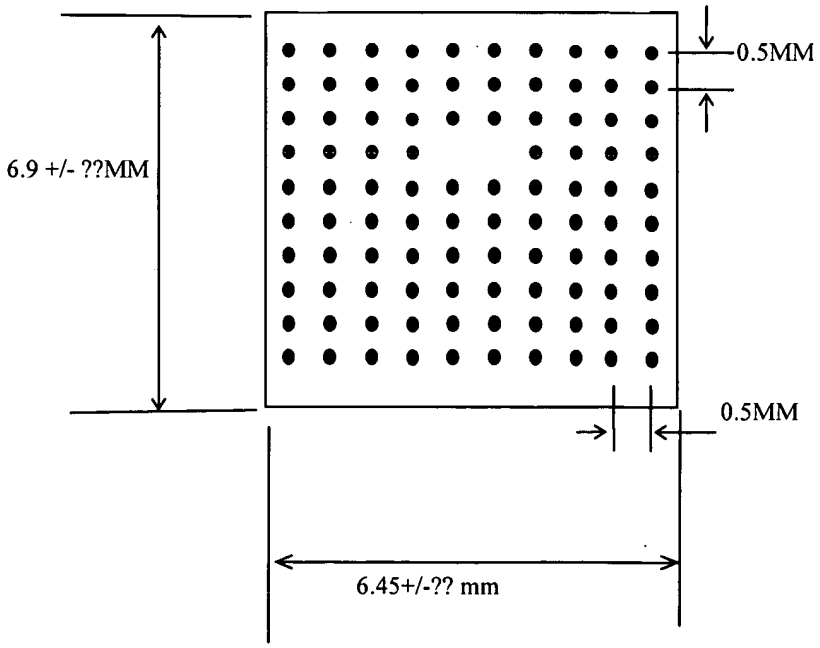
FOOTPRINT PATTERN *WS-0.5-12-98P*



STENCIL OPENING



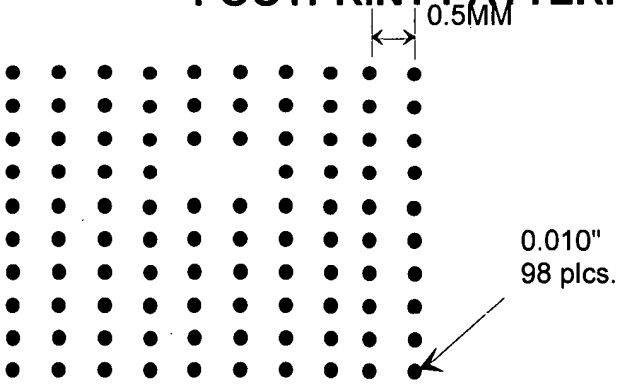
SUPPLIER PART SPECIFICATIONS BGA



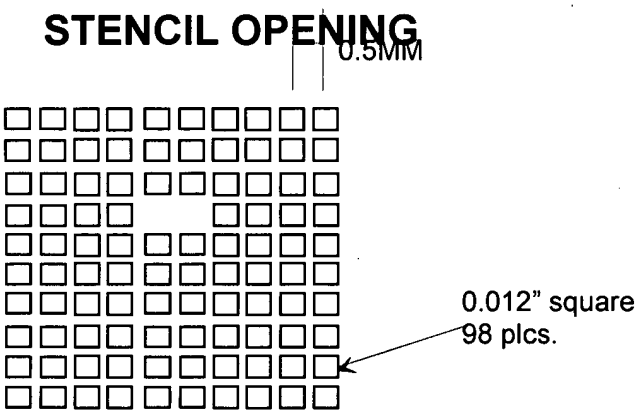
FOOTPRINT AND STENCIL OPENING
FOR 98 PIN BGA .5MM (FCT UltraCSP50 - 10 mil pad)

FOOTPRINT PATTERN

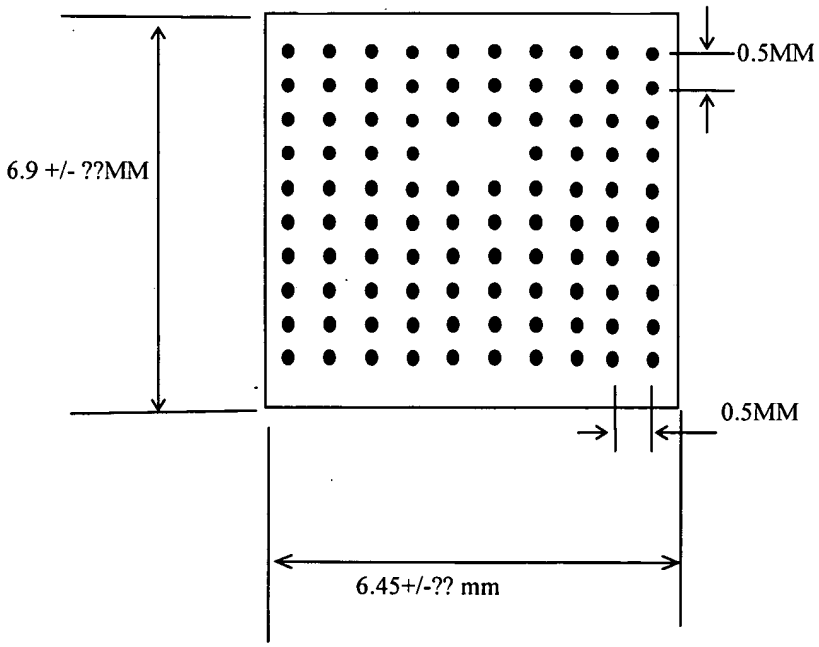
WS-0.5-10-98P



STENCIL OPENING

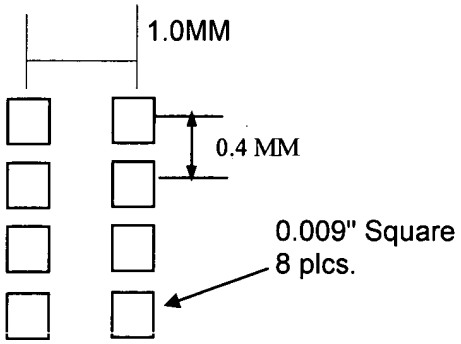


SUPPLIER PART SPECIFICATIONS BGA



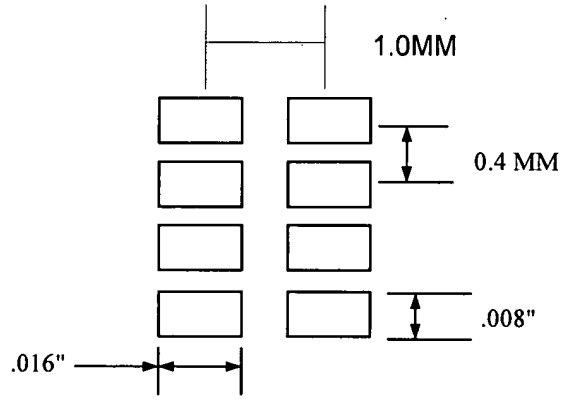
FOOTPRINT AND STENCIL OPENING
FOR 8 PIN DIEPACK 0.4MM PITCH (KOA-Speer)

FOOTPRINT PATTERN

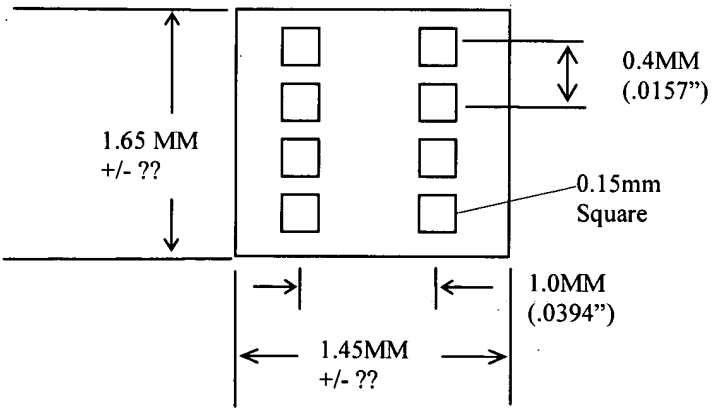


DP-1x0.4-8P

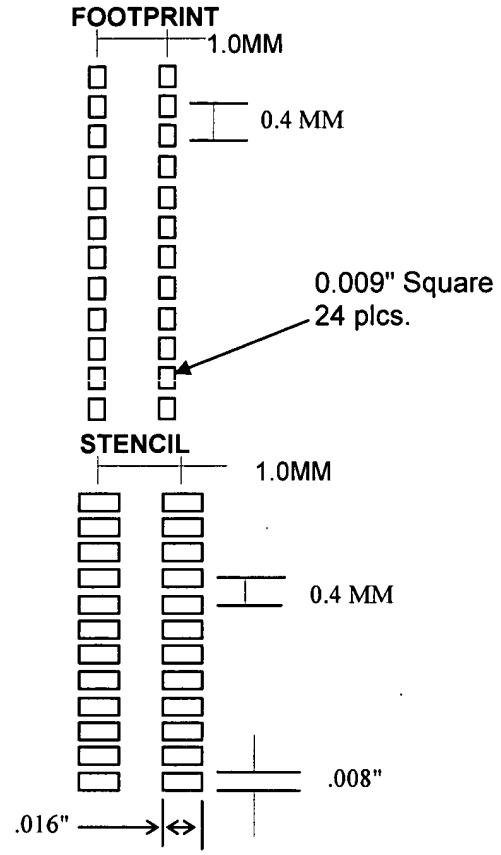
STENCIL OPENING



SUPPLIER PART SPECIFICATIONS CSP

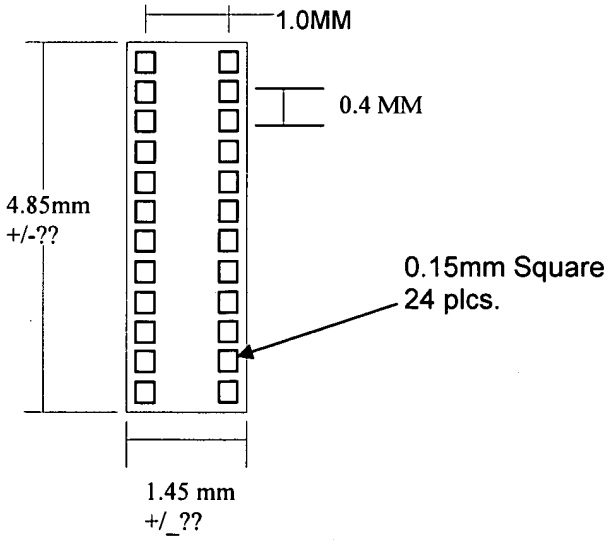


FOOTPRINT AND STENCIL OPENING
FOR 24 PIN DIEPACK 0.4MM PITCH (KOA-Speer)



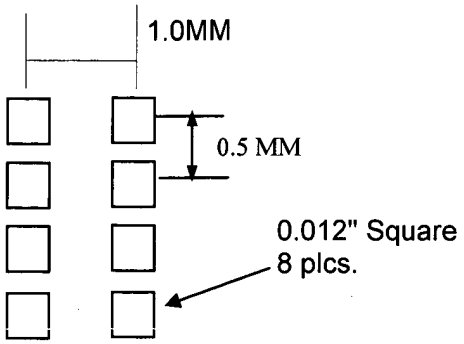
DP-1x0.4-24P

SUPPLIER PART SPECIFICATIONS CSP



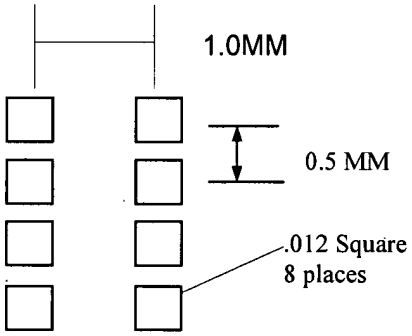
FOOTPRINT AND STENCIL OPENING
FOR 8 PIN DIEPACK 0.5MM PITCH (KOA-Speer)

FOOTPRINT PATTERN

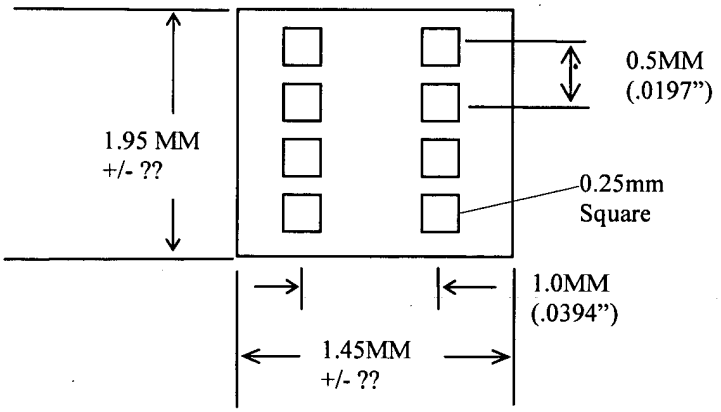


DP-1x0.5-8P

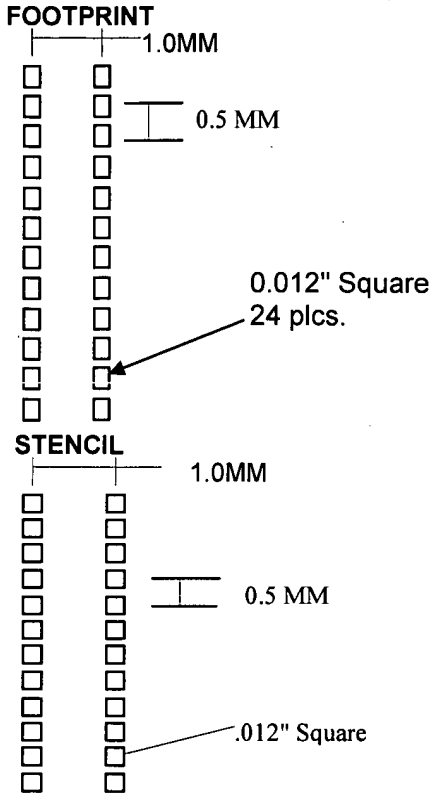
STENCIL OPENING



SUPPLIER PART SPECIFICATIONS CSP

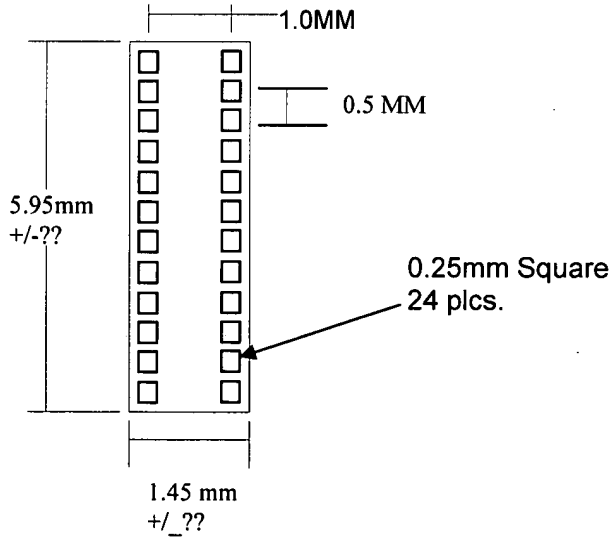


FOOTPRINT AND STENCIL OPENING
FOR 24 PIN DIEPACK 0.5MM PITCH (KOA-Speer)



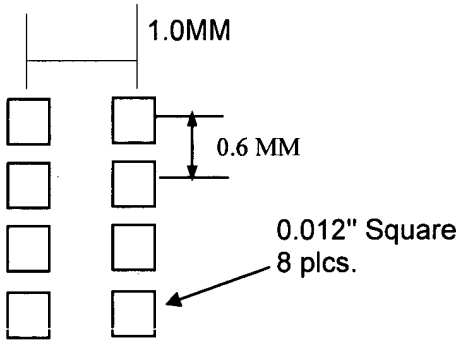
DP-1x0.5-24P

SUPPLIER PART SPECIFICATIONS CSP



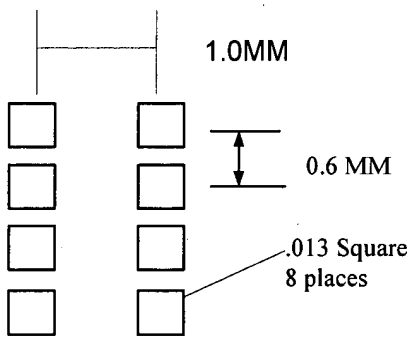
FOOTPRINT AND STENCIL OPENING
FOR 8 PIN DIEPACK 0.6MM PITCH (KOA-Speer)

FOOTPRINT PATTERN

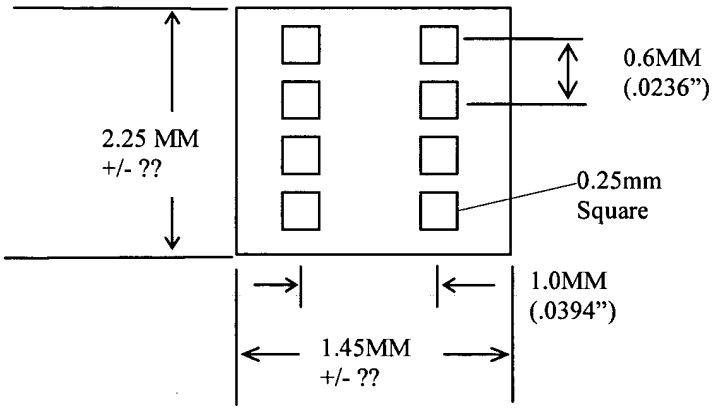


DP-1x0.6-8P

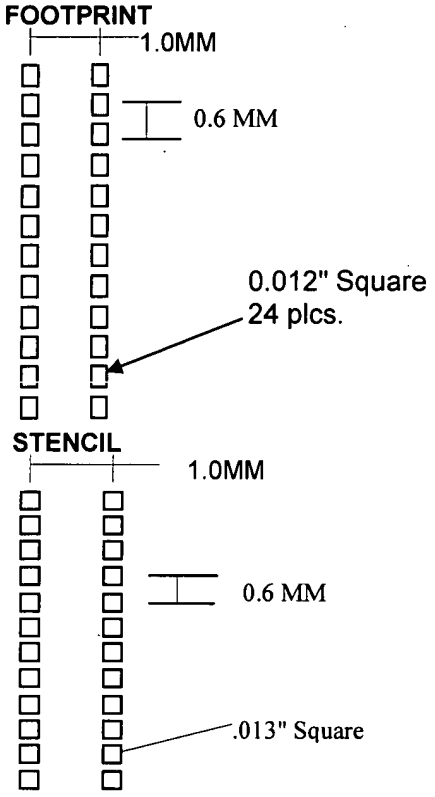
STENCIL OPENING



SUPPLIER PART SPECIFICATIONS CSP



FOOTPRINT AND STENCIL OPENING
FOR 24 PIN DIEPACK 0.6MM PITCH (KOA-Speer)



DP-1x0.6-24P

SUPPLIER PART SPECIFICATIONS CSP

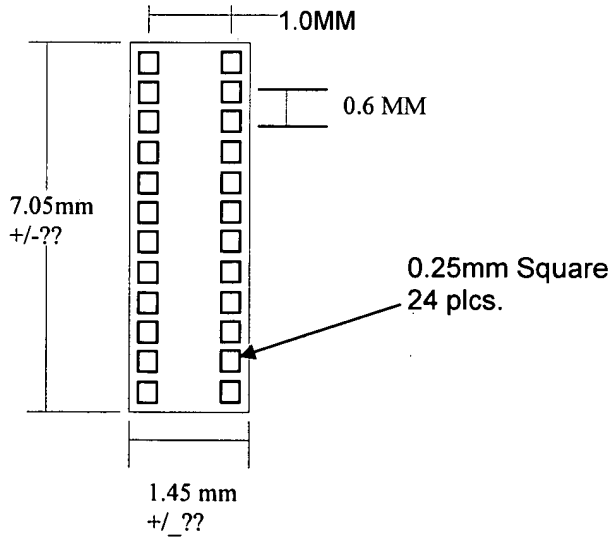


EXHIBIT C

Subj:	**proposal 09/940,749**
Date:	2/26/04
To:	annette.thompson@uspto.gov
File:	**G:\Scanner Output\c-503.PDF** (188876 bytes) DL Time (TCP/IP): < 1 minute

Examiner Thompson,

Attached is a proposed response for this case. Thanks for you time in discussing the case today.

I'll update to the format to the current version of the rules before filing.

Chris Maiorana
v 586-498-0670
f 596-498-0673
maioranapc.com

EXHIBIT D

Subj: **Re: proposal 09/940,749**
Date: 2/27/04
To: Annette.Thompson@USPTO.GOV

Isn't this what we discussed?

In a message dated 2/27/04 11:58:57 AM Eastern Standard Time, Annette.Thompson@USPTO.GOV writes:

> Dear Mr. Maiorana,
> I have considered the proposed response. Unfortunately, the response does not place this application in a condition for allowance. Therefore, the response if submitted would not be entered.
>
> Respectfully,
> Annette Thompson
> Primary Examiner
> Art Unit 2825
> (571) 272-1909
>
> > -----Original Message-----
> > **From:** ChrisMaiorana@aol.com [mailto:ChrisMaiorana@aol.com]
> > **Sent:** Thursday, February 26, 2004 4:34 PM
> > **To:** Thompson, Annette
> > **Subject:** proposal 09/940,749
> >
> > Examiner Thompson,
> >
> > Attached is a proposed response for this case. Thanks for you time in discussing the case today.
> >
> > I'll update to the format to the current version of the rules before filing.
> >
> > Chris Maiorana
> > v 586-498-0670
> > f 596-498-0673
> > maioranapc.com

EXHIBIT E

Subj: **RE: proposal 09/940,749**
Date: 2/27/04 3:20:49 PM Eastern Standard Time
From: Annette.Thompson@USPTO.GOV
To: ChrisMaiorana@aol.com
Sent from the Internet (Details)

Mr. Maiorana,

Partially. There is still more work to be done.

Annette Thompson
Primary Examiner
Art Unit 2825
(571) 272-1909

-----Original Message-----
From: ChrisMaiorana@aol.com [mailto:ChrisMaiorana@aol.com]
Sent: Friday, February 27, 2004 1:24 PM
To: Thompson, Annette
Subject: Re: proposal 09/940,749

Isn't this what we discussed?

In a message dated 2/27/04 11:58:57 AM Eastern Standard Time,
Annette.Thompson@USPTO.GOV writes:

> Dear Mr. Maiorana,
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>
> Respectfully,
> Annette Thompson
> Primary Examiner
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>
> > -----Original Message-----
> > **From:** ChrisMaiorana@aol.com [mailto:ChrisMaiorana@aol.com]
> > **Sent:** Thursday, February 26, 2004 4:34 PM
> > **To:** Thompson, Annette
> > **Subject:** proposal 09/940,749
> >
> > Examiner Thompson,
> >
> > Attached is a proposed response for this case. Thanks for you time in discussing the case today.
> >
> > I'll update to the format to the current version of the rules before filing.
> >
> > Chris Maiorana
> > v 586-498-0670
> > f 596-498-0673
> > maioranapc.com